Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Uneven temperature effect evaluation in high-power IGBT inverter legs and relative test platform design

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ARTICLE INFO

Article history:
Received 8 May 2017
Received in revised form 9 June 2017
Accepted 23 June 2017
Available online xxxx

Keywords:
Insulated gate bipolar transistor (IGBT)
High power compact IGBT
Switching characteristics platform
Junction temperature simulation method

ABSTRACT

This paper presents a high-power IGBT testing platform for uneven temperature conditions and its design criteria. Considering the influence of layout parasitic parameters on the measurement results, commutation rules and independent junction temperature control, a universal high-power switching characterization platform is built and operated. Importantly, it is capable of 3.6 kA current level test requirement, which can cover the largest current level for the state-of-the-art IGBT modules. To improve the test accuracy of double pulse test method, a compensation algorithm is proposed to eliminate the circuit power loss under high current test conditions. Moreover, in order to simulate the uneven junction temperature effects occurring in real life, the junction temperatures of inspected IGBT and freewheeling diode are controlled independently. Quantitative analyses of the switching characteristics for junction temperatures up to 125 °C are performed.

1. Introduction

Insulated Gate Bipolar Transistors (IGBTs) are widely used as active switches in many high-power industrial applications [1,2]. The demand for higher and higher converted power has pushed to enlarge continuously the capacity of single IGBT modules. The power rating has been extended to dozens of megawatts also in motor drives [3], and voltage and power in voltage-source converter high-voltage direct current stations (VSC-HVDC) have exceeded ±320 kV and 1000 MW, respectively, with modular multilevel converter topologies (MMCs) [4]. The single-phase converter station reported in [4] is made up of 1600 high-power IGBT modules; hence, a large number of high-power IGBT modules are needed.

In practice, the harsh working conditions worsen the reliability performance of high-power converters. According to an industrial survey, the semiconductor and solder failures in devices modules account for 34% of failures in the power converter systems, and that is the highest proportion in all failure cases. Moreover, nearly 60% of power device failures are temperature-induced [5]. On the other hand, the information provided in datasheets cannot fully reflect many important characteristics of candidate IGBT modules, such as switching behavior, robustness and reliability performance.

International Electrotechnical Commission (IEC) standard 60747-9 gives the standardized test methods for the extraction of static and dynamic electrical characteristics of discrete IGBTs. However, these test standards are implemented under standardized laboratory environment, while ignoring the matches between working environment and test configuration. Furthermore, these standardized laboratory test methods do not take into account the dependence of results on circuit parameters, operation conditions, and failure indicators in details [6]. In terms of high-power IGBTs test, the switching performances of IGBTs are always evaluated in an assembled prototype by using double pulse test (DPT) method [7]. In [8–10], the devices under test (DUT) in an assembled prototype are tested under various electrical stresses. Besides, the relationship among the switching losses, environmental temperature and loop parasitic inductors for press-pack IGBTs is studied in [11,12]. For an assembled power converter, the circuit parameters and mechanical structure are fixed. The test data reflect only the characteristics of DUTs in the established prototype. Users cannot screen the candidate IGBT modules from different manufactures and then optimize the related parameters. Besides, it is difficult to compensate the design flaws, which appear in the practical test. Concerning extreme stresses, many works have been presented so far. For instance, the static and switching characteristics of silicon-based IGBTs are evaluated at 200 °C in [13]. The clamped inductive turn-off failures are investigated under over current conditions in [14,15]. In [16,17], different failure mechanisms in IGBTs during unclamped inductive switching are studied.

In all the above studies, the characteristics of IGBT modules are evaluated and investigated under a uniform temperature environment. However, the temperatures of IGBT and commutation diode change with working conditions, such as power factor and, on top of it, they can differ significantly from each other. The above tests cannot

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http://dx.doi.org/10.1016/j.microrel.2017.06.054
0026-2714/

investigate the effects of a different diode temperature on the characteristics of IGBTs.

To address the above-mentioned issues, this paper presents synthetic design guidelines for a switching characterization test platform rated at 3.6 kA. Compared with previous test approaches, not only the dependence of switching characteristics on the circuit parameters, junction temperature, gate driver, can be tested, but also the uneven temperature effects can be investigated for the first time. The proposed universal test platform can cover the highest current level of IGBT modules. Moreover, an extension of [18], this paper proposes a compensation algorithm for circuit parasitics under high current test conditions, significantly improving the test accuracy of conventional double pulse test method. Furthermore, an independent temperature control method is proposed to investigate the uneven temperature effects on the diodes and IGBTs in high-power bridge legs.

2. Design rules of high power IGBT test platform

2.1. Testing principle

The half-bridge circuit with inductive load is widely adopted for the investigation of power devices. Furthermore, the half-bridge chopper circuit has also been used for short circuit and overcurrent evaluation under clamped inductive load [19]. In order to prevent the failure of DUTs, some extra power devices are usually included [20,21].

The switching characteristic test platform considering the parasitic parameters is plotted in Fig. 1. It includes a high voltage (HV) supply, capacitor bank C_d, film capacitor C_f, inductor load L_{load} and DUTs. L_{ESR} and R_{ESR} are the parasitic inductance and resistance of the capacitor bank. The commutation occurs between the upper anti-parallel diode D_M and lower IGBT switch S_M, which are taken from two separated high power IGBT modules. V_{dc} is the bus voltage, v_d is the diode D_M voltage, v_{ce} is the collector voltage, i_d is the diode current, I_L is the load current. i_c is the collector current of S_M, which is measured by the coaxial shunt. Because of the large size of capacitor bank, the parasitic inductors L_{s1} and L_{s2} are not negligible. Therefore, a film capacitor C_f is mounted on the bus bar.

The double pulse test (DPT) sequence for evaluation of switching characteristic is plotted in Fig. 2. Because of the huge demand for instantaneous energy, the required energy during the DPT process should be stored in the capacitor bank in advance. In order to ensure the safety of test platform, the whole DPT process needed to be separated from the power grid.

Firstly, the bus voltage V_{dc} needed to be charged to V_0. Then L_{load} is energized through switch S_M to the desired current in the first pulse.

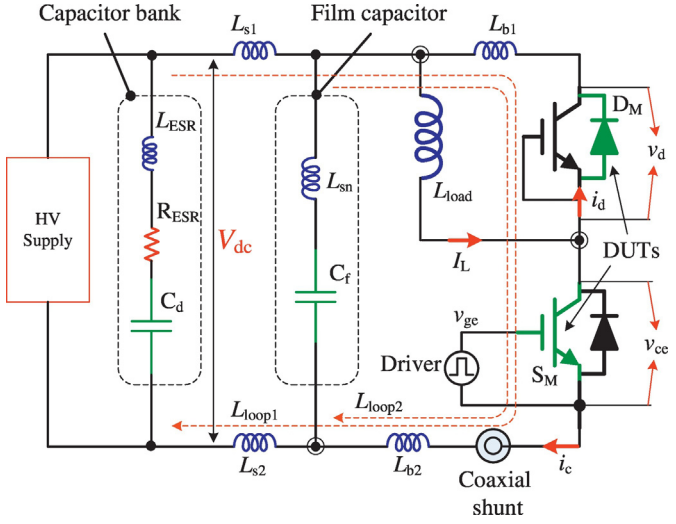

Fig. 1. Switching characteristic test circuit considering platform parasitic parameters.

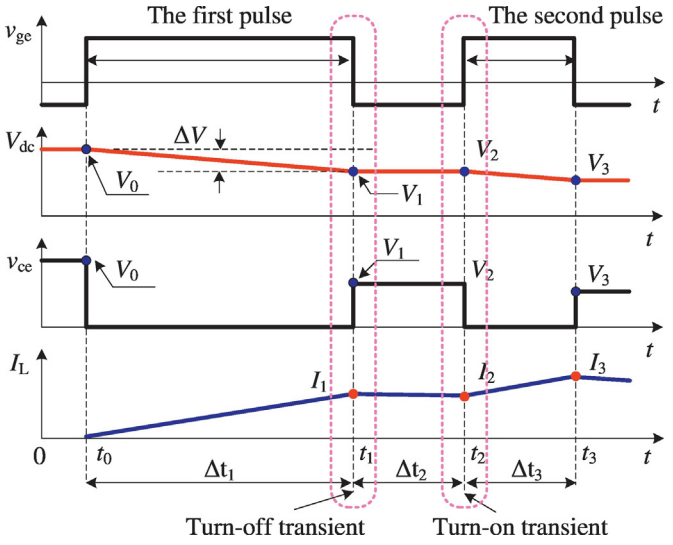

Fig. 2. Double pulse test sequence considering bus voltage drop.

At t_1, the collector current i_c reaches the desired current I_1 and the bus voltage V_{dc} falls to V_1 from V_0. Then I_L freewheels after S_M is turned off during Δt_2. When the second turn on pulse is applied to S_M at t_2, the turn-on and turn-off switching characteristics of S_M and D_M under the bus voltage V_2 and load current I_2 level can be captured at t_1 and t_2, respectively. Finally, when S_M is turned off at t_3, the whole DPT procedure is completed.

2.2. Synthetic design for capacitor bank and load inductor

In general, the huge energy needed in switching transient is only provided by the capacitor bank. The desired energy for DPT is approximately expressed as

$$E = \frac{1}{2}L_{load}I_L^2 = \frac{1}{2}C_d\left(V_0^2 - V_1^2\right) \tag{1}$$

For a DUT rated at V_{rating}, the maximum test voltage V_{max} should not exceed 70% V_{rating} for the safety of DUT [22]. In order to ensure V_{max} under the maximum current I_{max} test condition does not exceed 70% V_{rating}, The restrictions of L_{load} and C_d considering the test requirements can be determined by

$$\begin{aligned} &\frac{1}{2}L_{load}I_{max}^2 = \frac{1}{2}C_d\left[(V_{max}+\Delta V)^2 - V_{max}^2\right] \\ &\Rightarrow V_{max}+\Delta V = \sqrt{\frac{L_{load}I_{max}^2}{C_d} + V_{max}^2} < 0.7V_{rating} \end{aligned} \tag{2}$$

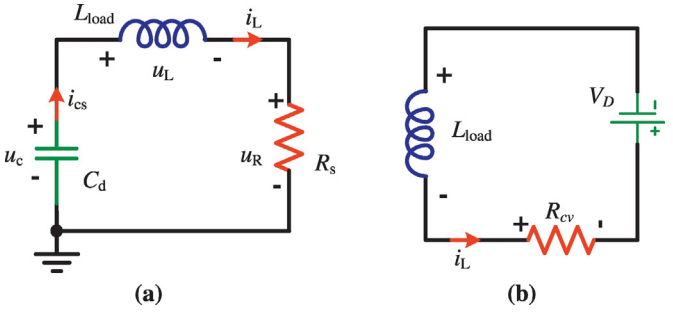

Fig. 3. Equivalent circuit diagrams during DPT process. (a) During Δt_1. (b) During Δt_2.

Please cite this article as: H. Luo, et al., Uneven temperature effect evaluation in high-power IGBT inverter legs and relative test platform design, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.06.054