Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Application of Scanning Capacitance Microscopy on SOI device with wafer edge low yield pattern

C.Q. Chen *, G.B. Ang, P.T. Ng, Francis Rivai, S.P. Neo, D. Nagalingam, K.H. Yip, Jeffery Lam, Z.H. Mai

Product, Test and Failure Analysis, Globalfoundries, Singapore

ARTICLE INFO

Article history:
Received 12 May 2017
Received in revised form 20 June 2017
Accepted 3 July 2017
Available online xxxx

Keywords:
SOI
SCM
Nanoprobing
Capacitance
Low yield

ABSTRACT

As semiconductor technology keeps scaling down, many advanced technology and process were applied in the semiconductor process. Especially for the application of IOT (internet of thing) technology, the low leakage and low power consumption product was the key component for this kind of application. SOI (Silicon-On-Insulator) wafer process is one of the advanced and important branches of the semiconductor manufacturing process. Its intrinsic advantage, low leakage and lower power consuming make it very suitable for personal communication device and IOT which match well with the application requirement. As is well known the SOI wafer is different form the normal bulk silicon wafer. The active sits on the silicon oxide insulator, which makes the final device separate from the substrate. Basically, all of the devices are floating on a nonconductive oxide layer. It comes with many challenges for process and analysis as compared with the conventional bulk silicon process.

The most conventional analysis method is not applicable in the SOI device such as the PVC (passive voltage contrast) and current image methodology which are a very powerful and important in the failure analysis.

In this paper, scanning capacitance is successfully used as the substitution of the PVC method. The SCM (Scanning Capacitance Microscopy) is a complicated process. Since all of the abnormality or physical change will affect the measured capacitance, then the capacitance signal will theoretically has many information with itself, including open, short and leakage. Through the detailed study, the contact level top-down SCM was successfully applied on the SOI unit. By proper setting of SCM bias condition, it can not only visualize the possible leaky location but also can reveal the possible path. Further nanoprobing and TEM (Transmission Electron Microscopy) have confirmed the SCM analysis.

1. Experiment and discussion

A low yield wafer with leakage failure mode was submitted for analysis. It has a wafer edge signature. The wafer map is shown as below, Fig. 1.

As is shown in the Fig. 1, the green color is a passed units, the other color are all failed units. Based on the data log, the majority failure mode is leakage JTAG (Joint Test Action Group) fail. The highly suspected failure circuit is the I/O circuit and JTAG interface circuit according to the failure and our understanding of the testing.

Based on the data log provided, the electrical measurement was conducted on the failed units as compared with the passed unit. DC (Direct Current) difference was found higher leakage (Iddq) in the bad unit as compared with reference units.

Since the electrical difference was found by the DC measurement, the static fault isolation was possible for this case. The conventional Fault isolation was conducted on the failed unit and exclusive hotspot was observed in the failed units as compared with reference unit, Fig. 2.

As is shown in the Fig. 2, hotspot was observed in the I/O circuit of the bad unit, but no spot was observed in the reference unit.

Subsequently, conventional layer by layer PFA (Physical Failure Analysis) was performed on the spot location. No abnormality was found until the contact level. Then the suspected layer was pointed to FEOL (Front End of Line) process, but further failure analysis is impossible to proceed on the unit since the hot spot coverage is micrometer range. PVC cannot work on this kind of unit and nanoprobing is also not applicable in this kind of case due to the big coverage of the hotspot [1,2]. Even nanoprobing still need the narrow down of the suspected structure to be probed. Since all of the conventional FA (Failure Analysis) methods have failed in this kind SOI device, Scanning Capacitance Microscopy was proposed.

Fig. 3 shows the transistor capacitance schematics. Although is quite complicated, but any physical change, including open, short and leakage, can affect the measured capacitance theoretically. Then it is possible for SCM to catch the possible defect location if the bias condition was proper set.

* Corresponding author.
E-mail address: Changqing.chen@globalfoundries.com (C.Q. Chen).

http://dx.doi.org/10.1016/j.microrel.2017.07.014
0026-2714/

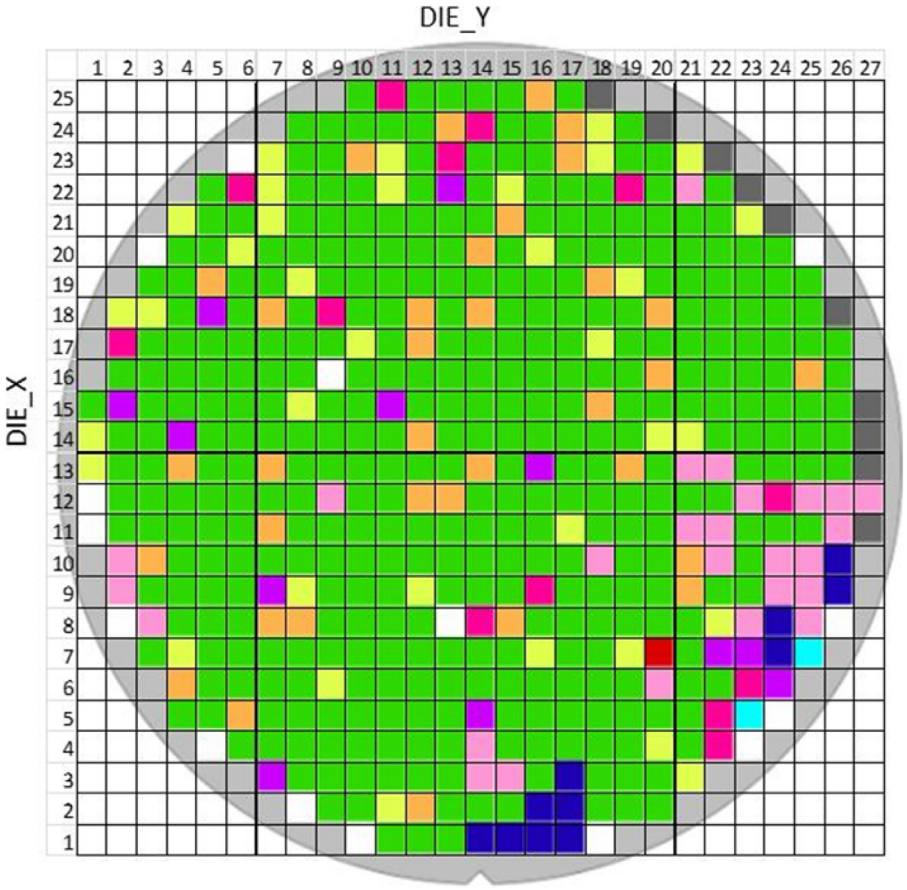

Fig. 1. Wafer map of the issue, green color is the passed unit, the other colors are all failed unit.

With this on mind, the question is Can we use SCM to do the top-down analysis at contact level? The contact level capacitance value is a lump sum result. It is a combination of junction capacitance, well-to-substrate capacitance and stray capacitance. But we think the lump sum result will be affected if some abnormality happened on the structure. If an apple-to-apple comparison was applied, it is also possible for us to find some difference.

With this assumption, the AFP (atomic force probing) SCM methodology was applied on the contact level electrical analysis. As is shown in the Fig. 4, the SCM scanning was conducted on the spot location by proper adjust the bias condition. Fig. 3a is the topography of the spot location and Fig. 3b is the SCM image with the proper bias condition setting. Since the SCM is a complex process, it detects the dC/dV value of the scanned area. That means the capacitance change rate is critical in the image visualization. So it is critical to adjust the bias frequency and voltage in the SCM imaging step.

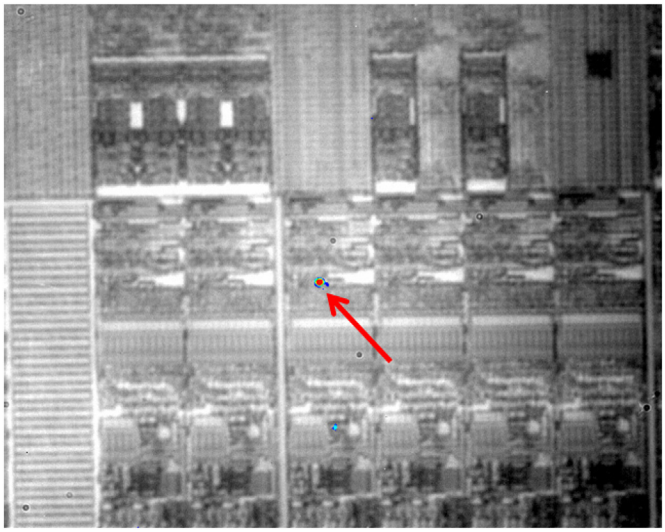

Fig. 2. Image of static fault isolation analysis.

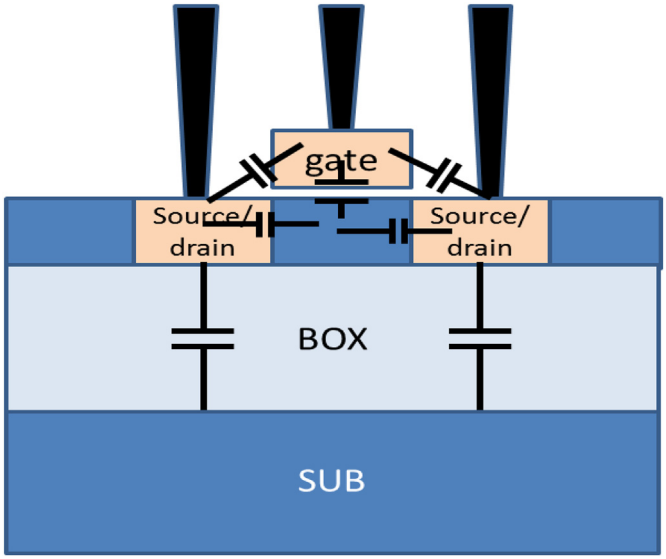

Fig. 3. Capacitance schematic of the SOI transistor.

Please cite this article as: C.Q. Chen, et al., Application of Scanning Capacitance Microscopy on SOI device with wafer edge low yield pattern, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.07.014