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Analysis of ageing effects on ARTIX7 XILINX FPGA

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ABSTRACT

FPGAs are considered as an attractive alternative to ASICs, thanks to their reconfigurability and their low development costs. However, since they are the first experiencing new technology nodes, their ability to tackle VLSI ageing mechanisms is crucial, especially in critical applications such as space and avionics ones. This work aims to understand ageing degradation on FPGAs. An experimental approach is adopted in order to characterize the effects of degradation on FPGAs Look up tables (LUTs). Different stress conditions were tested to accelerate ageing process and identify the mechanisms behind. Ageing tests have been executed on a total of 17 FPGAs belonging to Artix7 XILINX family. Results show that Negative-Bias Temperature Instability ageing damage is the main cause of timing degradation on the studied FPGAs.

1. Introduction

Negative-Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time-Dependent Dielectric Breakdown (TDDB) and electromigration (EM) are key reliability issues in MOSFETs. These ageing mechanisms manifest themselves as an increase in the threshold voltage as well as a reduction in drive current, leading to performance degradation at circuit level.

Given the growing importance of FPGA, many works have been devoted to ageing effects on this kind of device [1–4]. In Ref. [5], the authors used a transistor-level circuit of the LUT, in order to predict ageing behaviours and propose mitigation techniques on FPGAs. Although modeling is a practical approach, without the precise knowledge of the physical architecture and transistor parameters of the LUT, as well as ageing models of the process technology, the results will be biased and will not reflect the realistic ageing effects. The work in Refs. [1] and [2] has investigated accelerated-life testing to characterize ageing degradation on commercial FPGA.

In this work, the approach proposed in Ref. [1] is enriched with more test conditions in order to understand the dependency of different ageing mechanisms on external and internal stress conditions. Moreover, real tests on recent FPGA family targeting sub-nanometer technology have been performed, which enable further improvement in reliability estimation methodology such as FIDES [6].

This paper is organized as follows. In Section 2, we review the most important ageing mechanisms in VLSI circuits. Section 3 presents the different tests implemented to characterize the ageing degradation of the FPGA. Measurement results are discussed in Section 4. Finally, concluding remarks are drawn in Section 5.

2. Background-ageing mechanisms

The main ageing mechanisms described in the literature over the last several decades are: Negative-Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time-Dependent Dielectric Breakdown (TDDB) and electromigration (EM).

NBTI is a static mechanism affecting PMOS transistors when a negative field is applied to its gate potential. It is caused by the accumulation of a hole-population in the bulk underneath the oxide interface, resulting in interface states generation and hole trapping phenomena [7,8] . NBTI accelerates at elevated temperature and manifests itself as an increase in the threshold voltage (V_{th}) as well as a reduction in drive current of the PMOS transistor, leading to performance degradation at circuit level. A power-law model to time and an Arrhenius law describing the relationship to temperature, are generally used to describe the V_{th} shift due to NBTI [9,10] :

$$\Delta_{V_{th}} \alpha \quad exp\left(\frac{-E_a}{KT}\right) t^n. \tag{1}$$

Recent works have shown partial recovery of the damage as soon as the NBTI stress is stopped [11]. Hence, for pulsed stress, PMOS transistor undergoes alternate stress/recovery phases. The resulting degradation is known to be duty cycle dependent while the frequency dependence is not yet fully understood and shows conflicting results in the literature [12,13] .

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Hot-Carrier Injection damage happens under high source-drain bias (V_{DS}) and optimal gate-source bias (V_{GS}) conditions [14]. Due to high lateral electric field near the drain, carriers moving along the channel in MOSFET are no longer in thermal equilibrium and are "hotter" than the surrounding lattice. They gain additional energy allowing them to overcome the potential barrier of the gate dielectric and inject into the gate oxide. Like NBTI mechanism, HCI leads to transistor parameters shift over time resulting in slower switching. But, while NBTI occurs in static conditions, HCI takes place in dynamic CMOS operation, i.e. when transistors switch. Hence, HCI degradation increases with the switching activity of the transistors. The temperature dependence of the HCI is not yet conclusive. For a long time, Hot-carrier phenomena are known to accelerate in low temperature. However, in Ref. [15], authors explain that this is the case of old technologies using long-channel transistors and large stress voltages. They added that for recent process technologies, the temperature dependence is reversed as the operating voltage are scaled and MOSFET channel length are shortened.

Like NBTI, TDDB occurs in the standby mode. It is caused by an accumulation of traps in random positions inside the gate dielectric, resulting in a conductive path between the gate and the substrate. The damage induces a significant leakage current which increases the power consumption and results in a slower switching. This Soft-Breakdown (SBD) can progress to cause a catastrophic failure of the device known as a Hard-Breakdown (HBD).

Electromigration is a mechanism affecting the interconnects. Due to the high current density, metal ions migrate over time in the direction of the electron current inducing voids at one end and hillocks at the other end of the metal line. As a result, EM can induce open circuits (due to voids) or short circuits (due to hillocks).

3. Ageing test implementation on FPGAs

As ageing mechanisms have a negative impact on the circuit performance, Ring Oscillators (ROs) were chosen as ageing effect sensors and the variation of their frequencies serve to characterize the ageing degradation on FPGAs. Fig. 1 shows the structure of the RO-based sensor. The `Stress` signal can be a static signal (DC0, DC1) or an AC signal generated by the PLL of the FPGA, whose frequency and duty cycle are fixed by the user. The `Mode` is a control signal sent by the user through the UART to the CUTs: `Mode` at logic value '0' corresponds to the *stress mode*, where the sensor is in an open loop. In that case, the `Stress` signal passes through the LUTs constituting the RO and the counter downstream provides its frequency. Comparing the frequency of the `Stress` signal provided by the counter with the one expected from the PLL serves to check that no ageing problem have occurred in the counter block. With `Mode` at logic value '1', the sensor operates as a ring oscillator (i.e. *normal mode*) and the counter generates the corresponding frequency.

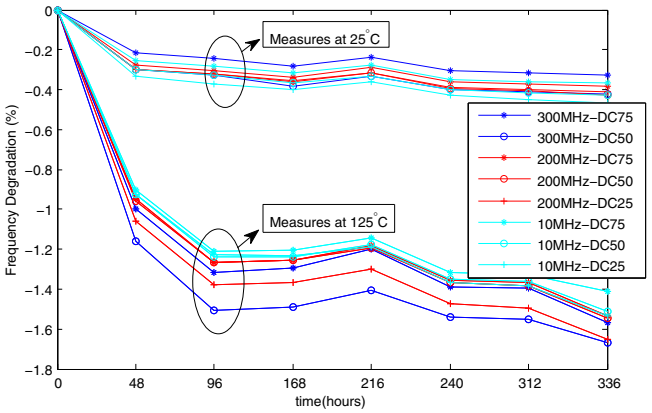

Fig. 2. Impact of the duty cycle of the stress signal on the frequency degradation of ROs.

The Digilent Basys3 board, featuring a TSMC-28 nm XILINX ARTIX7 FPGA has been used in this work. Ageing tests have been executed on a total of 17 FPGA. Different ROs have been considered (different LUT configurations, different number of LUTs per RO and different stress signals). In each FPGA, a set of 200 CUTs were manually placed to be sure that they are physically identical. And 20 tests, which corresponds to 10 CUTs per test, are performed. Hence, the degradation due to a certain test conditions is the mean of the degradation of the 10 circuits under this test. Tests are carried out using different temperatures(0 ° C, 35 ° C and 125 ° C). High temperatures are produced by a heater plate and low temperatures are obtained using a Peltier device. Both temperature suppliers are directly attached to the FPGA. The aim is to accelerate ageing mechanisms and extract some model parameters such as activation Energy (E_a).

4. Results

The aim of the experimental results analysis is to investigate the impact of different parameters on the ageing degradation.

4.1. Impact of the duty cycle of the stress signal

Fig. 2 shows the degradation due to different AC stress signals with different duty cycles. For the same stress signal frequency, the duty cycle of 25% degrades more than the duty cycle of 50% which

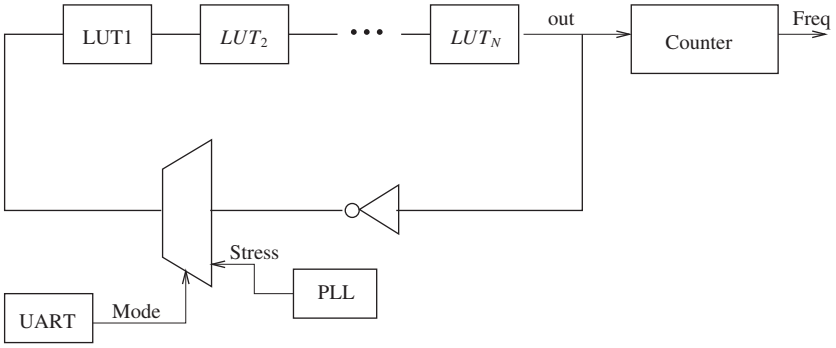

Fig. 1. RO-based sensor structure.