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Technologies for Heterogeneous Integration - Challenges and chances for fault isolation

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ABSTRACT

The evolution of electronic devices for Integrated Circuits following Moore's law is one of the fastest industrial development speeds – and still far too slow for the rapid increase of performance requirements demanded by Internet of Things, growing cloud computing and other innovations in microelectronics. 2D scaling following Moore's law may come to an end from now on. But, the explosion of data collection, exchange and storage will require a dramatic increase of operating frequency, requiring very low power, low latency, sensors & actuators. All these aspects will have consequences for contactless fault isolation (CFI) that go far beyond the challenges of the past, being mostly imaging resolution and operating frequency with a given basic material of silicon. The presentation will check the readiness of CFI for the scaling still in expectation by assessing optical probing using visible light. Heterogeneous Integration aspects like radio frequency operation, the influence of new materials for actives, optical interconnects, ultra-shallow TSV will be checked for risks and new opportunities of CFI. Together with test, reliability and security requirements, a new world of electronic devices is envisioned and options are presented how challenges to CFI may be mastered by taking chances for new concepts of debug and failure analysis.

1. Introduction

The evolution of electronic devices for Integrated Circuits as we know it through Moore's law, is one of the fastest industrial development speeds – and still far too slow for the requirements of the next generation internet.

The ITRS roadmap – in the past the milestone setter for Moore's law in microelectronics has been predicting 2014 technology nodes down to 2.5 nm for 2025 [1]. On the way to this ambitious technology development, it seems more and more unrealistic to realize such small dimensions with further cost reduction. There is probably not much further 2D-scaling in expectation so SIA discontinued the roadmap update in 2016 with no direct statement how much lower than 10 nm nodes will go in the future [2]. This can be considered as the end of Moore's law.

On the other hand, the electronic devices need to master a number of challenges that require a more drastic performance increase than Moore's law has ever predicted. The main drivers of the necessary technology revolution are:

- Internet of Things (IoT),
- Migration of data to cloud, and
- Consumerization of data and access.

This statement has been edited as ITRS 2.0 [2], considering that solutions for the challenges listed above can only come from new concepts and new materials. The IEEE CPMT (Components, Packaging, and Manufacturing Technology Society) is now editing a Heterogeneous Integration Roadmap (HIR) [3]. Both documents are more looking ahead than real milestone setting. They identify a list of key challenges to master the performance requirements:

- Radio frequency operation (10–100× data rate),
- Low power, low latency at higher performance,
- Devices must move closer (3D integration),
- Photonic interconnects,
- Built in self test (BIST),
- Assured Reliability and Hardware Security, and
- Cost needs to decrease further.

Contactless fault isolation (CFI) is the key process to identify critical performance areas when first silicon goes to test and debug needs to be done as well as in failure analysis if devices fail at customer in valid reliability condition. This publication will assess the readiness of CFI for the remaining ITRS roadmap in the next chapter. The following chapters will discuss the challenges and chances of CFI while 3D integration and increase of data rate, testing and security aspects are drastically changing everything.

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2. Fault isolation for further scaling

Following the traditional ITRS roadmap [1], we can expect a maximum decrease of technology node by a factor of 2–3 in the coming 10 years, bringing FinFETs to ca 5 nm nodes. The circuit debug and failure analysis (FA) today is handled using optical interaction - based contactless fault isolation (CFI) techniques applied through chip backside in near infra – red (NIR) regime. The big advantage of NIR is the relative transparency of silicon, so sample preparation is pretty convenient. With the best solid immersion lens (SIL) equipment, the resolution can go down to ca. 170 nm. Due to [5], this resolution is sufficient to do fair CFI on technology nodes down to 10 nm with a device pitch of 64 nm. In [4] is shown that the device pitch is decreasing to ca 40 nm for 5 nm nodes. Fig. 1 is showing the CFI readiness for the technology nodes and their respective pitches for the pure NIR case and the NIR with SIL support. The gray shading shows that for 10 nm nodes the coverage of NIR + SIL is still there but fading. Further scaling would require other CFI solutions. As long as CFI techniques remain based on optical interaction, further improvement of resolution can only be provided if the optical wavelength is reduced. Table 1 is demonstrating which innovation is necessary to reduce wavelengths. A resolution increased by a factor of 2 will require different SIL material and drastic bulk Si thinning down to challenging single micrometers. Shorter wavelengths require more glass-like materials with a considerable loss in n. Then, the drastically decreasing transparency would require bulk Si thickness of few nanometers, which makes this a very unrealistic way to go.

But, with the VIS + SIL solution of 550 nm wavelength, CFI seems to meet the scaling that is expected by the remaining bandwidth of Moore's law. FinFETS with such small geometries would provide important performance advantage by shrinking in size. But the gain of performance is by far not sufficient for the needs of the expected data rate explosion, Here, other technologies will join in. CFI concepts of the future will have to take those aspects into account as well.

3. Heterogeneous Integration

Thinking of operative bandwidths 100 GHz and higher, the active devices on chip level are not the limiters of bandwidth. The main losses are global interconnects. Fig. 2 describes that the delay of CMOS nodes and local interconnect nets will decrease with miniaturization, whereas Global Nets will limit performance with smaller geometries. If everything could move closer, the required data rate could be managed, even on silicon technologies. This, of course, is even more important for the system on chip (SoC) or the package. The top priority of technology innovation must therefore be on 3 D integration (Section 3.1). Then, RF signals cannot be fed from external testers anymore, most testing has to be integrated on the chip (Section 3.2). Once test function is on chip, it may of course run more or less continuously allowing for more precise reliability and security assessment (Section 3.3). Especially with the end of CMOS scaling, more and more non-silicon materials will be involved – the reason to call this technology development phase "*Heterogeneous Integration*". When data rate requirements will increase clock rate well above 100GHz, the only Global Net concept may be photonic interconnects (Section 3.4), a complete paradigm shift of electronic device operation. In the end, active devices will consist of the materials with highest carrier mobilities (Section 3.5). Section 4 will discuss how all these changes might influence IC fault isolation techniques as needed for debug and failure analysis and how these new chip concepts may help getting this job accomplished.

Table 1
Wavelength of optical CFI technique, required SIL material and resolution (after [4]).

Wavelength [nm]	SIL material	n of SIL mat.	Resolution [nm]	Absorption depth in Si [μm]
1064	Si	3.5	152	<300
650	GaP	3.3	98	3
550	GaP	3.4	81	1.5
440	SiC	2.7	81	0.13
330	C	2.5	66	0.012

3.1. 3D integration

The bandwidth of through silicon vias (TSVs) is very much depending on their aspect ratio [7,8]. The key for fast connections between SoC chips is a thin bulk. With a TSV height of only a few microns, bandwidth of 100 GHz and beyond is within reach. With such shallow dimensions, vertical active devices are in sight. Vertical nanowire devices have already been demonstrated [9,10]. And, the vertical dimensions of a chip stack becomes similar to today's interconnect stack of a single chip.

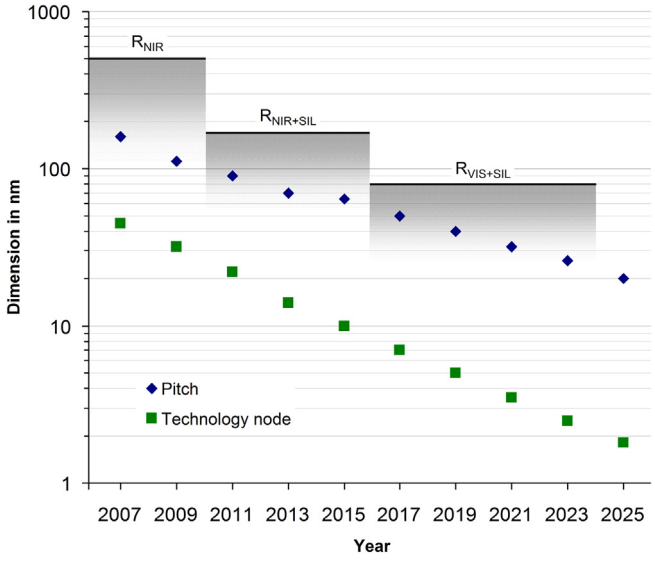

Fig. 1. Technology node generations with their FET pitch sizes according to ITRS roadmap [1]. Gray areas indicate fault isolating capability in real world IC debug with NIR and NIR + SIL based on [5] and adapted for VIS + SIL (after [4]).

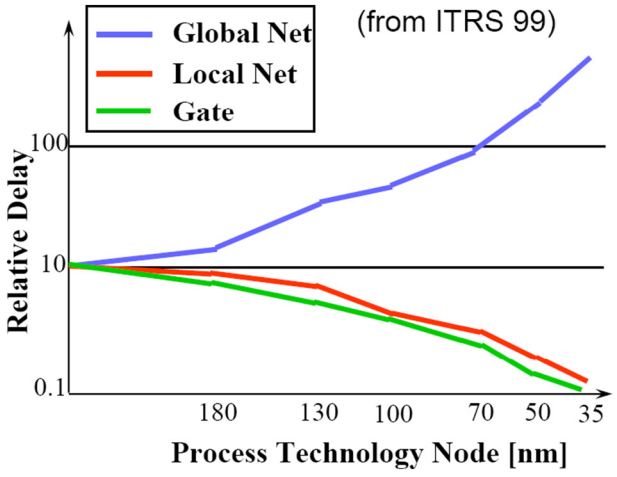

Fig. 2. Miniaturization reduces delay of CMOS active devices (Gate) and short interconnect lengths (Local Net). Long interconnects (Global Net) do not scale with feature sizes and become circuit speed limiters (ITRS roadmap 1999, after [6]).

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