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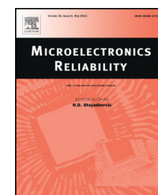

Lock-in thermal laser stimulation for non-destructive failure localization in 3-D devices

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ABSTRACT

We report a new non-destructive method to localize interconnection failures in 3-D devices. The scanning optical microscopy (SOM) technique is based on lock-in thermal laser stimulation (LI-TLS) and uses thermal waves to non-destructively map the current path in a 3-D device. We validate the method with test structures and show how the magnitude and phase of a propagating thermal wave may provide valuable 3-dimensional information on the failure location. We apply the technique on a short failed chain structure in a four level chip stack with an intensity modulated laser as a thermal wave injector and the structure under test as a detector. We confirm our results by physical failure analysis through a selective cross sectioning process.

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1. Introduction

As the semiconductor industry is approaching the end of traditional Moore's Law scaling, the emergence of three-dimensional (3-D) integration is gaining increased momentum. To keep up with the consumer demand for smaller, faster electronics with extended and new functionalities, the industry will rely more and more on 3-D interconnection schemes [1]. 3-D integration does not only enable a higher interconnect density, shorter wire lengths, and reduced chip size, but also allows for heterogeneous integration. The through-silicon via (TSV), wafer bonding, and wafer thinning are key technologies for 3-D integrated devices. Two common types of products which make currently use of TSVs are DRAM memory stacks [2] and camera sensors [3].

The increased complexity of 3-D devices poses a challenge for failure analysis (FA), in particular, being able to precisely localize buried defect sites within the vertically interconnected 3-D package is becoming ever more challenging. The latest developments on FA techniques for 3-D packaging have recently been reviewed by Altmann and Petzold [4], Li et al. [5], and De Wolf [6].

Non-destructive failure localization in multi-chip devices is desirable as the complex build-up often hinders or prevents direct access to the interconnections under test, which may inevitably lead to the destruction of the overall device functionality. Non-destructive techniques may not only reduce the analysis time and resources, but also increase the success rate, as physical failure analysis (PFA) methods have typically longer turnaround times and may induce additional defects within the device.

As both optical and electron beam based defect localization techniques have been extremely valuable to the FA engineer due to unique interactions of photon and electron beams with the integrated circuit (IC), the scanning optical microscope (SOM) and scanning electron microscope (SEM) have become standard tools in FA laboratories since the early 1990′s. However, these techniques have provided so far only limited applications to 3-D fault isolation (FI), mainly because many beam based electrical fault isolation (EFI) techniques require direct optical and electron access to the interconnections under test. This is often difficult to achieve due to the abundance of opaque layers and interconnects within the 3-D device.

Until now, only a limited number of non-destructive EFI techniques exist for localizing interconnection failures in complex 3-D devices. The most promising EFI techniques for 3-D include: magnetic field imaging (MFI) [7], lock-in thermography (LIT) [8], electro optical terahertz pulse reflectometry (EOPTR) [9], and high frequency TSV analysis [10]. We recently reported a scanning optical microscope (SOM)-based technique named light-induced capacitance alteration (LICA) for detecting and localizing interconnection failures in TSV structures for 3-D integration [11]. This LICA technique is based on photon probing of interconnect capacitance to localize interconnection failures in TSV structures. The technique allows rapid, efficient, and non-destructive fault isolation of interconnection failures at the wafer level, and is applicable to passivated devices.

It is noted that thermal laser stimulation (TLS) has already proven to be successful for 3-D defect localization in the BEOL of a single chip. In 2007, Reverdy et al. reported a laser beam modulated OBIRCh technique whereby a dynamic laser source was applied on a 90 nm CMOS BEOL structure to obtain 3-D information (thus including depth information) of the defect by studying the temporal behaviour of the alteration of the thermally stimulated current [12]. It has also been shown that by using a

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pulsed laser in combination with a lock-in amplifier, a gain in S/N ratio can be achieved and an improvement in spatial resolution is possible by reducing the heat spreading in the chip [13]. Whilst the technique has proven to be valuable for 3-D defect localization in BEOL structures, it has never been applied to 3-D devices to the best of our knowledge.

In this paper, we propose and demonstrate lock-in thermal laser stimulation (LI-TLS) as a non-destructive EFI method for localizing interconnection failures in 3-D devices. The technique non-destructively maps the current path by inducing a thermal wave in the 3-D device under test with an intensity modulated laser. To explore the feasibility of the method, we demonstrate the technique on a four level chip stack with built-in temperature sensors to assess the ability to excite and detect thermal waves in a 3-D stacked device and the spatial resolution of the measurement. We then apply the technique on a short failed TSV daisy chain in a four level 3-D stacked IC (SIC). Finally, we confirm our results by physical failure analysis (PFA) through a selective cross sectioning process.

2. Lock-in thermal laser stimulation (LI-TLS) for 3-D electrical fault isolation (EFI)

The TLS term refers to three major static mapping techniques that rely on the interaction of the infrared (IR) beam and IC: optical beam induced resistance changes (OBIRCh), thermally induced voltage alteration (TIVA), and Seebeck effect imaging (SEI). OBIRCh was developed by Nikawa and Tosaki in 1993 [14], whilst TIVA and SEI was developed by Cole in 1998 [15].

The principle behind OBIRCh and TIVA is to create a local thermal gradient with a spatially confined laser source to induce a resistivity variation, $\Delta\rho$, in a heated metal element according to Eq. 1.

$$\Delta\rho = \rho_0 * \alpha_{TCR}(\Delta T) \quad (1)$$

where ρ_0 is the metal resistivity, α_{TCR} is temperature coefficient of resistance of the metal and ΔT is the temperature variation induced by the laser. The resulting thermally induced resistance variation (ΔR) is monitored by measuring the power consumption of the device. In particular, the detection scheme depends on the applied biasing method (i.e. TIVA measures the voltage at a constant current, whilst OBIRCh measures current at a constant voltage). By correlating the detected variation in power consumption with the laser spot location, information on the origin of the resistance variation, and hence the failure location can be obtained.

2.1. Thermal wave propagation for 3-D failure localization

Thermal-wave physics has been of importance in material science for the study of semiconductor materials and devices (e.g. quantitative thin-film measurements) [16]. Thermal waves occur whenever there is periodic heat generation and heat flow in a medium. A common method to induce a thermal wave in a medium involves the absorption of the energy from an intensity modulated optical beam. A 3-D FA technique that relies on the detection of thermal waves is lock-in thermography (LIT). The first demonstration of this technique on a 3-D device was by Schmidt et al. in 2008 [8]. Since then, this technique has been widely adopted by the industry as a tool for accurate localization of resistive opens and electrical shorts in packaged 3-D devices. The technique is based on detecting and imaging the related hot spots generated by small amount of dissipated electrical power at the defect site. Defect localization in 3-D is enabled by measuring the amplitude and phase image of the thermal response. The amplitude image of the measured thermal response provides a quantitative measure of the temperature change at the defect to the surrounding and can be used for defect localization in the plane, whilst the phase image, which relates to the phase shift between the electrical excitation and the thermal response at the imaged surface, contains information on the defect depth. The phase shift is related to the travelling time of the heat flow in the device. Of note is that our method relies on the same underlying thermal wave physics of LIT, but the injection and sensing of the amplitude and phase of the thermal wave in the device is done differently. Our proposed approach uses a laser as a thermal wave injector and the actual structure under test as the detector, compared to LIT whereby the electrical defect in the structure under test behaves as the thermal wave injector and an external infrared camera as the detector. A key feature of our approach is that is can be carried out on a standard SOM tool, thereby effectively extending the tool's functionality for 3-D FA. However, we expect that both techniques complement each other, with each having their own unique advantages and disadvantages for detecting and localizing specific failures. This will have to be explored in future studies.

2.2. Principle of lock-in thermal laser stimulation (LI-TLS) for failure localization in 3-D devices

We propose and demonstrate a method to non-destructively map the current path in a 3-D device through thermal laser stimulation. The injection of the thermal waves in the device is achieved with laser light, whilst the actual structure under test is used as a thermal wave detector. A lock-in scheme with pulsed laser excitation is required to induce a periodic thermal wave inside the 3-D device under test. Noteworthy is that a near-infrared (NIR) laser operating below the Si bandgap energy (1.1 eV) is typically used for TLS to avoid the photocurrent generated by inducing electron-hole pairs in the substrate, which could mask the thermal effect in the IC. Furthermore, a NIR laser also provides the opportunity for backside analysis due to the transparency of Si to infrared radiation.

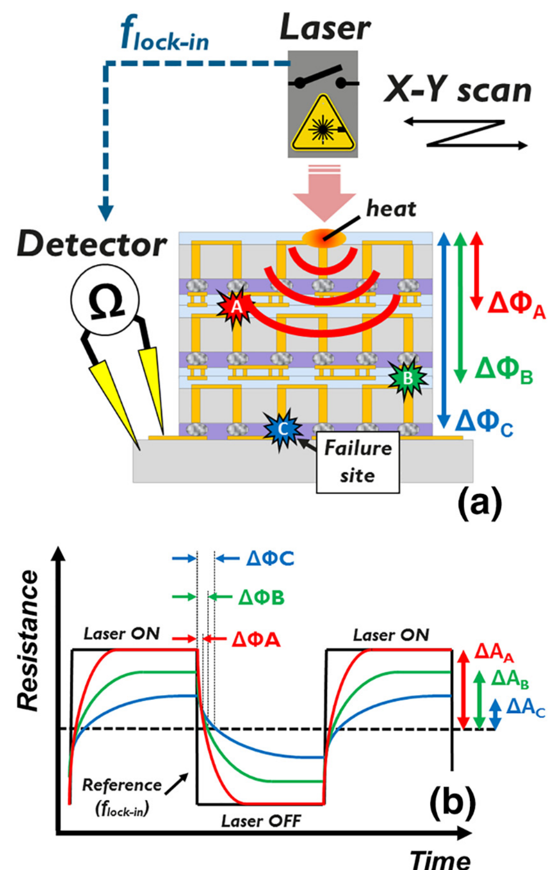

Fig. 1. (a) Cross-sectioned schematic of a four-level die stack illustrating LI-TLS for 3-D failure localization; (b) Corresponding thermal response for failures A, B, and C, indicating the change in measured amplitude and phase shift.

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