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Circuit simulation assisting Physical Fault Isolation for effective root cause analysis

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ABSTRACT

In this study, the PFI (Physical Fault Isolation) was assisted with the analog circuit simulation to provide insight into the device performance under the failed condition and the failure mechanisms. This approach allows us to choose and apply the right PFI technique to find the failure root cause in a very time effective manner and propose the failure mode hypothesis. Accordingly, as an alternative to the conventional circuit modification approaches a backside PLS (Photoelectric Laser Stimulation) based technique was applied to the suspicious analog block. In this technique, a laser with the wavelength in the NIR (Near Infrared) range stimulates the analog circuit block at the transistor level and changes the device electrical state from fail to pass. Consequently, we could evaluate the circuit behaviour at failed condition and verify the failure. In this manner, the competent combination of PFI and analog circuit simulation successfully leads us to the corrective action to improve the circuit design and overcome the inevitable fabrication process variation.

1. Introduction

The rapid growth of the semiconductor industry requires highest level of quality with fastest product development process at a lowest cost. In such complex manufacturing process, failures are inevitable and may occur at any phase during design, fabrication process, test or qualification. Therefore, quick FA (Failure Analysis) process and immediate corrective actions have become the essential part of this industry. To meet these requirements, we need powerful failure analysis tools and techniques and as well the technical knowledge to implement the most effective technique. In this manner, the information about the device performance obtained by circuit simulation can improve the FA process significantly. The simulation assisting PFI (Physical Fault Isolation) benefit FA engineers to organize the failure analysis, and approach the root cause more efficiently. The analog simulation and circuit analysis helps to interpret the PFI results and consequently narrow down the suspicious areas that might be the failure root cause. In the complex FA cases, the FA engineer may use the feedback information from the circuit simulation to approach the failure root cause by employing more effective electrical setup or PFI technique to stimulate and consequently isolate the defective area. To overcome a design problem or weakness, the circuit simulation assisting PFI is the most effective approach. In such cases, the PFI engineer should work in close collaboration with the designers to exchange the results and lead the analysis process effectively to detect the design weakness and declare the corrective action. For simple analog circuits, this should be preferably done within the FA-Lab when the PFI engineers learn to deal themselves with the analog circuit simulation tools. This approach would reduce the FA cycle time drastically.

In this work, we demonstrate the importance of the circuit analysis and the analog simulation in a frame of a case study based on the FA performed on a device failed during the first silicon. The results of PFI analysis and the circuit simulation provide a better understanding about the device performance under the failed condition and the state of the suspicious circuit at the transistor level. Furthermore, this approach helped us to develop an alternative non-destructive FA technique to edit the affected analog circuit block which was failed due to the combination of the fabrication process variation and circuit design weakness.

For this purpose, we employ a PLS (Photoelectric Laser Stimulation) based technique to change the electrical state of the DUT (Device under Test) from fail to pass. Using this non-destructive method, we prove successfully the proposed failure mode hypothesis in practice. Finally, we highlight the significant assistance of the analog circuit simulation to PFI procedure to find and apply the corrective action to the circuit design.

2. Sample

The DUT is a highly integrated PMC (Power Management Chip) with a wide selection of supply domains, mobile peripheral and interface drivers optimized to support mobile application processors. The PMC device is mainly used to manage and control the power distribution

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flow and direction in the host system. The DUT is a mixed signal IC (Integrated Circuit) with WLCSP (Wafer Level Chip Scale Package).

3. Physical Fault Isolation (PFI)

DUT shows a relatively high static current consumption of about 80 μA in a specific operational state where the current should be in the nA range. The PFI was realized on an iPHEMOS (inverted Photon Emission Microscopy) Hamamatsu system by biasing the device under the static failed electrical condition to find abnormal backside EMMI (Emission Microscope)/PEM (Photon Emission Microscopy) or OBIRCH (Optical Bam Induced Resistive Change) signal response.

No abnormal OBIRCH signal response was observed on the failed device. However, as it is depicted in Fig. 1, an abnormal EMMI signal was detected on the failed device at elevated supply voltage (VDD). The EMMI signal, circled by red, is superimposed on the micrograph image.

3.1. Circuit analysis assisting PFI

The schematic/layout correlation with the abnormal EMMI spot (Fig. 1) reveals that the EMMI signal is originated from the "level shifter reset" block of a DC-DC Buck converter. The circuit is partially represented in Fig. 2. The confidentiality regulation does not allow us to publish the whole circuit.

The 'level shifter reset' block is connected to two separate ground rails 'Vss' and 'VSUB'. The latter one is the substrate ground. The circuit is supplied with two different power supply rails, namely 'dvdd' and 'VDD-HI'. The first one is connected to the main power supply rail and the latter one is the voltage to supply the drivers and the logic of the corresponding blocks at the output. In comparison to a normal level shifter, this block is supplied with an input pin, namely 'res_n', which enable the circuit to reset the corresponding VDD domain in the output. Four important internal nodes are also defined, namely 'aa', 'cc', 'Inb' and 'Outb', which are connected to drain of N1 and N5, gate of N5, gate of N1 and input of the output stage, respectively.

Table 1 shows the truth table of the 'level shifter reset' block. 'VDD-HI' represents the high state at output ('Out') of the block. The high state at input ('A' and 'res_n'), and internal nodes ('Inb', 'aa', 'cc', 'Outb') are represented by 'dvdd'. As it is showed in Table 1, when the 'res_n' is at low state the output resets to '0', and consequently the VDD rail of the corresponding circuit blocks at the output disables.

In this case study, the failed device works in the specific operational mode with the 'res_n' biased at low state. Based on the truth table in Table 1, the output 'Out' should be in this condition at low state. Therefore, in the output stage P4 and N4 transistors should be 'Off' and 'On', respectively. These functional states would guarantee that the level shifter is in the reset mode and the blocks connecting to its output are disabled.

The obtained EMMI signal correlates at the layout and schematics with the NMOS transistor (N4) at output stage of the block (Figs. 1 and 2). This result indicates that the N4 transistor is operating in the saturation mode, although based on the circuit analysis it should be in the 'On' state. The circuit analysis shows that, in this operational state the power supply ('dvdd') of the suspicious block is floated. Consequently, the gates of two NMOS transistors, N1 and N5, are floated. Thus, the state of the gates and subsequently the channels underneath are not very predictable, and any process variation could drive these two transistors in different state. Therefore, in some devices both NMOS and PMOS transistors in the output stage operates in the saturation mode and so the overall DUT current consumption increases. The obtained strong EMMI signal in Fig. 1 at the output stage confirms the proposed device operation.

Yield data analysis reveals that the failure rate is very low and just a limited amount of the devices failed under this specific condition. Therefore, we can conclude that a design weakness accompanying with a manufacturing process variation should be the failure root cause.

3.2. Circuit simulation

We performed circuit simulation in Virtuoso ADE (Analog Design Environment) to evaluate the proposed hypothesis. The "Cadence®

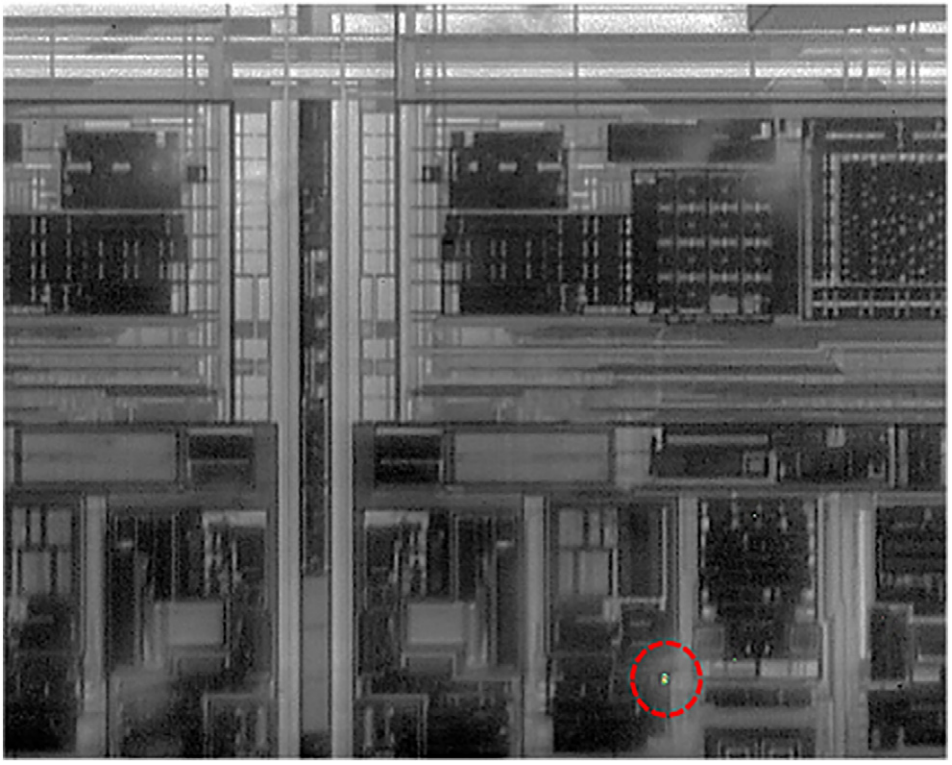

Fig. 1. The EMMI signal (circled by red line) is localized by applying the electrical condition to bias the failed device in the specific operational mode.