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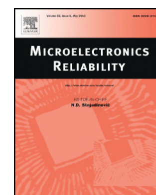

Failure analysis methodology on donut pattern failure due to photovoltaic electrochemical effect

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ABSTRACT

This paper described a low yield case which resulted in a donut shape failing pattern. It also described a scenario where static fault localization is ineffective and a systematic problem solving approach based on symptoms, induction, hypothesis and verification was engaged to resolve the issue with understanding on the root cause and the failure mechanism. The low yield is due to residual light in the dilute HF clean tool which results in photovoltaic electrochemical effect on the exposed metal, through via holes, connecting to large PN junction. This results in subsequent resistive via formation and analogue failure.

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1. Introduction

Failure analysis (FA) is an integral step for the development and manufacturing of semiconductor integrated circuits (IC) and fault localization is the most crucial step in the entire FA cycle. In the wafer foundry industry, fault localization using photon emission microscopy [1,2] and laser induced techniques [3], like Thermal Induced Voltage Alteration (TIVA) and Optical Beam Induced Resistance Change (OBIRCH), are effective for localizing a whole host of resistive opens and shorts in the logic circuitries and memory arrays that results in static leakages and yield loss.

However, these techniques are not effective for analogue circuitry failure as the simple biasing scheme of VDD and VSS is often insufficient to trigger the device into the failure mode. Although dynamic fault localization could be a feasible approach, it requires additional resources in packaging the failure dies and customer support on the device test board and test program to exercise the packaged parts to the failing mode. These resources and supports are usually not available. An alternative approach would be to perform wafer level dynamic fault localization [4]. This requires an extremely stable Scanning Optical Microscope system that is capable of holding the 12″ wafer for high pin count direct tester-docked wafer level probing using production probe card [5,6]. This allows direct fault localization analysis to be done using the wafer sort test conditions. However, due to cost avoidance or IP confidentiality reasons, this capability may not be enabled for every product. Thus, with limited information and test support available, alternative approach need to be engaged to resolve the analogue failure encountered in foundry. In this paper, a systematic problem solving methodology based on symptoms, induction, hypothesis and verification was engaged to

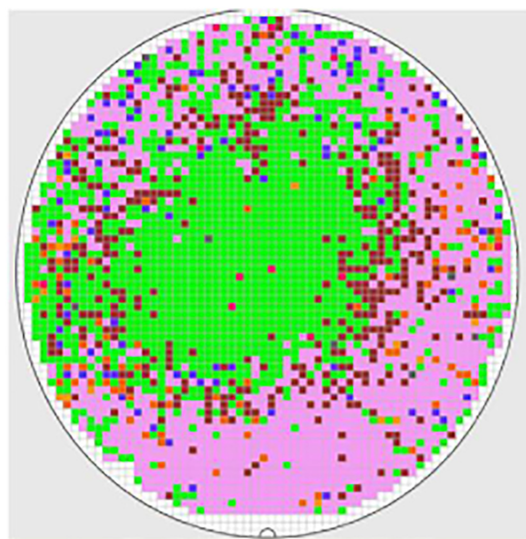

Fig. 1. Typical wafer sort failing map of the affected wafers.

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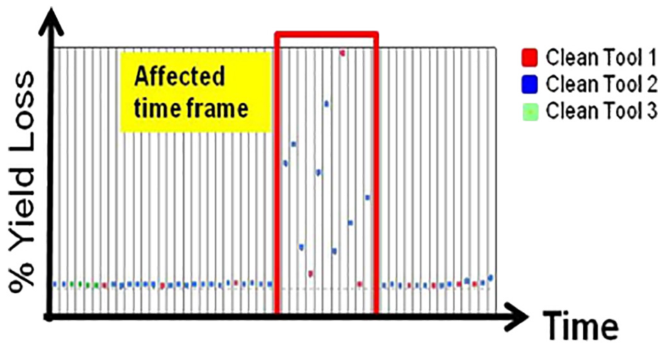

Fig. 2. Correlation of yield loss with clean tool at metal 2 DHF clean step.

Fig. 3. Via 1 – metal 2 dual damascene process flow.

resolve an analogue failure with an understanding on the root cause and the failure mechanism.

2. Results and discussions

2.1. Symptom 1: failing pattern

Wafer fabrication encountered a low yield issue with distinct donut pattern analogue failure across several devices. A typical wafer sort failing map was shown in Fig. 1 to illustrate the donut pattern with green colour representing passing dies and pink colour sites representing

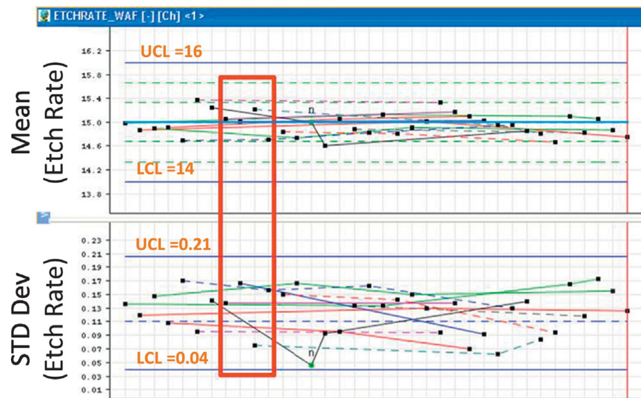

Fig. 4. Control chart of the HF Etch rate in the affected chamber. No abnormal etch rate observed.

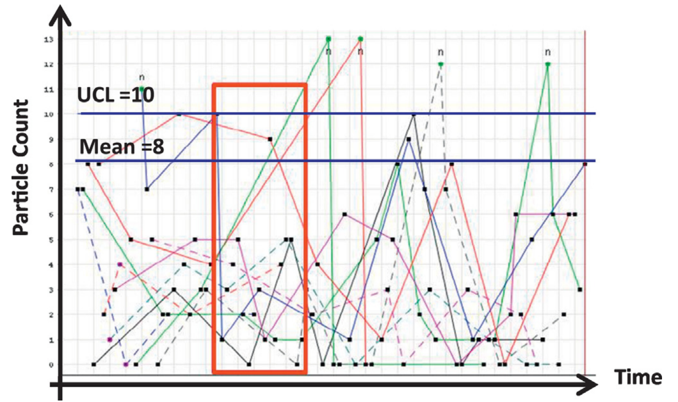

Fig. 5. Control chart showing the particle count. No abnormal particle count of the HF detected in the affected chamber.

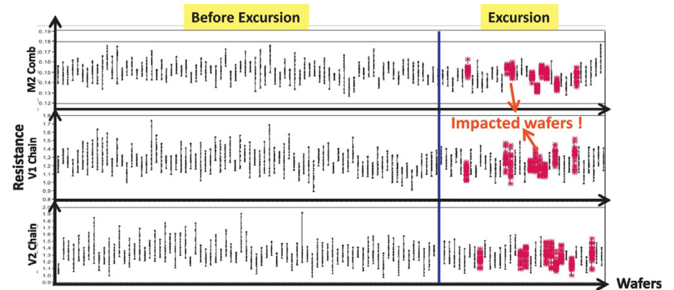

Fig. 6. Via1 chain/Metal 2 comb/Via 2 chain resistance were comparable between good and bad wafers.

dies with analogue failure. As all the affected devices were of the same 65 nm technology node and impacted wafers exhibited similar donut pattern and analogue failing mode, this suggested that there was no device sensitivity and the low yield was related to generic process tool issue.

Table 1
Summary table of the first 3 failure symptoms and its inductions.

	Symptoms	Inductions
1st Symptom	Wafer sort map	Generic process/tool issue
	All 65nm devices & similar donut pattern on affected wafers	General 65nm process/tool issue. Not device sensitive
2nd Symptom	Tool commonality	Intrinsic process issue
	▪**Wet clean tool at M2 DHF step** with chamber commonality ▪Chambers showed **no etch rate and particle count anomaly**. ▪**No queue time correlation**	▪Possibly failed structure: **Metal 1 → Metal 2** ▪Cause of failure is **NOT due to contamination or abnormal etch of DHF**
3rd Symptom	ET and Wafer Sort Results	Structural Dependent
	•ET showed **no anomaly**. •**Analog functional failure only**	•**Not a gross issue** •Failure was structural specific → sensitive to **big capacitor /WELL/active**

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