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Reliability of 100 nm AlGaN/GaN HEMTs for mm-wave applications

M. Dammann [a,*], M. Baeumler [a], V. Polyakov [a], P. Brückner [a], H. Konstanzer [a], R. Quay [a], M. Mikulla [a], A. Graff [b], M. Simon-Najasek [b]

[a] Fraunhofer Institute for Applied Solid State Physics, Tullastrasse 72, D-79108 Freiburg, Germany
[b] Fraunhofer Institute of Microstructure of Materials and Systems, , Walter-Hülse-Strasse 1, D-06120 Halle, Germany

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ABSTRACT

The effect of gate metallization and gate shape on the reliability and RF performance of 100 nm AlGaN/GaN HEMTs on SiC substrate for mm-wave applications has been investigated under on-state DC-stress tests. By replacing the gate metallization from NiPtAu to PtAu the median time to failure at $T_{ch} = 209$ °C can be improved from 10 h to more than 1000 h. Replacing the PtAu T-gate by a spacer gate further reduces the degradation rate under on-state stress, but decreases the current-gain cut-off frequency from 75 GHz to 50 GHz. Physical failure analysis using electroluminescence and TEM cross-section revealed pit and Ni void formation at the gate foot as the main degradation mechanisms of devices with NiPtAu T-gate. High resolution EDX mapping of stressed devices indicates that the formation of pits is caused by a local aluminium oxidation process. Simulation of the stress induced changes of the input characteristics of devices with NiPtAu gate further proves the formation of pits and Ni voids.

1. Introduction

Due to its high breakdown voltage and saturation velocity GaN power amplifiers offer high power operation in the *E*-band (60–90 GHz) and W-band (75–110 GHz) for mobile communication, millimetre wave imaging and automotive radar applications [1]. In order to reach high frequency power performance, field plates have to be removed to reduce parasitic capacitances. By comparing 100 nm long T-gate devices to gate terminated field plate devices Burnham et al. found that there is a trade-off between RF performance and reliability due to the electrical field peak increase at the gate foot [2]. T-gate devices achieve twice the operating frequency compared to field plate devices, but the T-gate devices degrade faster under DC operation due to gate sinking [2]. In order to improve long term stability without field plate, the effect of gate metallization and gate morphology has been investigated in this work. RF performance and on-wafer reliability of devices with T-gate and spacer gate using NiPtAu and PtAu gate Schottky contacts have been compared. Failure analysis using electroluminescence (EL) and TEM has been used to understand the faster degradation rate of devices with NiPtAu gate. Accelerated DC stress tests of packaged single stage amplifiers have been performed to determine the extrapolated median life time of the T-gate technology process.

* Corresponding author.
E-mail address: Michael.dammann@iaf.fraunhofer.de (M. Dammann).

2. Experiment

2.1. Technology

The processing of the different gate shape technologies of the 100 nm AlGaN/GaN HEMT devices used in this study was described by Brückner et al. [3]. As listed in Table 1 two different gate shapes with either PtAu or NiPtAu gate metallization have been compared. All wafers were epitaxially grown by MOCVD on 4 in. SiC substrate and had a similar sheet resistance as listed in Table 1. A focused ion beam (FIB) cross-section of the spacer gate is shown in Fig. 1a where the gate length is defined by optical lithography. The spacer gate starts with an optical definition of a 500 nm large opening in a sacrificial layer. By anisotropic depositing of a further passivation layer, the gate-foot opening is shortened to the intended gate-length and etched isotropic for the opening. For the T-gate shown in Fig. 1b the gate shape is defined by a three layer resist e-beam lithography process

2.2. Reliability tests

The device under test for the on-wafer stress test is a $2 * 50$ μm wide device with equal gate drain and gate source distance of 0.7 μm. The on-state stress test was performed at $V_d = 20$ V and a base plate temperature of 150 °C. The gate voltage was adjusted to keep the drain current

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Table 1
Sheet resistance, gate shape and gate metallization of the 4-inch wafers used in this work.

Wafer	R_{sheet} (Ω/sq)	Shape	Metallization
1	508	T-gate	NiPtAu
2	515	T-gate	PtAu
3	605	Spacer	NiPtAu
4	520	Spacer	PtAu

constant at 225 mA/mm. The estimated channel temperature is 190 °C based on micro Raman spectroscopy measurements [4]. Intermediate measurements were done at stress temperature to monitor the degradation of important electrical parameters such as the saturation current I_{dss} at $V_d = 5$ V and $V_g = 1$ V. For the reliability tests of packaged devices an 8 finger single stage amplifier with a total gate width of 0.48 mm has been used. The device was mounted in a commercial available package using silver filled epoxy resin. The packaged reliability stress test was performed at $V_d = 15$ V, $I_d = 300$ mA/mm and a channel temperature of 209 °C. For the intermediate measurements the device was cooled down to a base plate temperature of 50 °C.

2.3. Failure analysis

A packaged four finger, prematched transistor of wafer 1 with a total gate width of 0.18 mm has been chosen for failure analysis. The device was stressed in on-state at $V_d = 15$ V, $I_d = 300$ mA/mm for 200 h at $T_{ch} = 175$ °C. The electroluminescence (EL) has been measured before and after DC stress under off-state, subthreshold and on-state conditions. For physical failure analysis using high resolution TEM two cross section lamellas have been prepared by FIB [5].

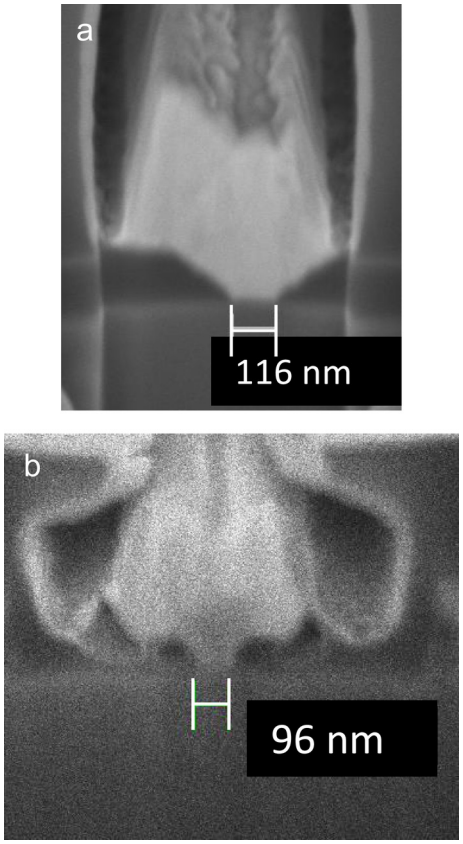

Fig. 1. FIB cross-section of spacer gate (a) and T-gate (b).

3. RF performance results

The maximum oscillation frequency, f_{max} and the current-gain cut-off frequency, f_t have been extracted from S-parameter measurements. As shown in Fig. 2 the average f_t and f_{max} values are reduced for the spacer gate due to the higher parasitic capacitance value. The T-gate wafer with PtAu gate has the best switching performance with f_t around 75 GHz and f_{max} around 110 GHz. The f_t of the PtAu spacer gate is around 50 GHz.

4. Reliability results

4.1. On-wafer reliability

Fig. 3 shows that the degradation rate of devices with NiPtAu gate is faster compared to devices with PtAu gate. Based on a failure criterion of −5% of IDSS, the time to failure at $T_{ch} = 190$ °C is around 20 h for NiPtAu, whereas the extrapolated time to failure of devices with PtAu exceeds 1000 h. The spacer gate with PtAu gate is even more stable than the T-gate.

4.2. Packaged reliability tests

The reliability improvement by replacing the NiPtAu T-gate by a PtAu T-gate was confirmed by long term stress tests shown in Fig. 4. The lifetime at $T_{ch} = 209$ °C increases from 10 h to an extrapolated median time to failure of more than 1000 h as shown in the upper part of Fig. 4a. The lower part of Fig. 4a shows an initial negative threshold voltage for both gate metals and during stress a stronger positive threshold voltage shift of the NiPtAu T-gate compared to the PtAu T-gate.

Fig. 4b and c show the input characteristic and the subthreshold slope during stress for both gate metals. The initial subthreshold slope of the NiPtAu is substantially larger compared to the PtAu gate. The subthreshold slope at Ud = 5 V before (after) stress is 0.52 V/decade (0.57 V/decade) for the NiPtAu gate, whereas it is only 0.22 V/decade (0.27 V/decade) for the PtAu gate.

5. Failure analysis results

5.1. Electrical characterization

As shown in Fig. 5 the prematched transistor from wafer 1 (NiPtAu T-gate) used for failure analysis shows a reduction of the gate and

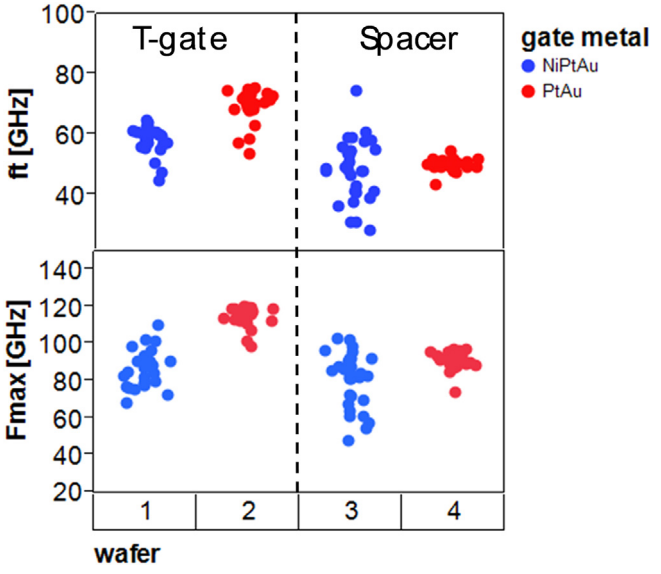

Fig. 2. Maximum oscillation frequency f_{max} and the current-gain cut-off frequency f_t.

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