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Experimental study of the instabilities observed in 650 V enhancement mode GaN HEMT during short circuit

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ABSTRACT

The paper presents the results of an experimental analysis of the short circuit behaviour of 650 V GaN power HEMT. It is shown that the DUTs exhibit two kinds of failure. A first failure mode involves large dissipated energies and can be attributed directly to the increase of the local temperature in the device. The second failure mode is less attributable to local thermal increase and it is proposed that it is associated with instabilities due to charge-field phenomena taking place in the device at high voltage. The paper shows that 650 V GaN power HEMTs are affected by high frequency oscillations which appear in the SC waveforms as it happens in the short circuit of the IGBTs.

1. Introduction

GaN Power HEMTs (High Electron Mobility Transistors) are very interesting devices both in their depletion (normally on) and enhancement (normally off) versions. In fact, the former are widely used as very performing active devices in high frequency RF applications [1,2]. Depletion mode GaN Power HEMTs with high voltage blocking capabilities can be also employed in switching power converters where they are mounted in a cascode configuration together with low blocking voltage power MOSFET to achieve very performing high voltage (~600 V) switches [3]. The introduction of the enhancement mode GaN Power HEMTs has been very well welcomed in the power electronics applications due to their very good performances in terms of on state and switching energy losses [4]. Recently, high voltage enhancement mode GaN Power HEMTs rated at 650 V have been made commercially available [5].

Despite many research efforts have been dedicated to the reliability issues of GaN Power HEMTs [6] only little attention has been paid to the behaviour of these devices in Short Circuit, SC, which instead is a main concern in any power electronics applications [7]. Some papers have been dedicated to the SC behaviour of the cascode combination of MOSFET and depletion mode GaN Power HEMTs [8,9,10]. The interpretation of the experimental results seems to be quite contradictory in these papers. In fact, the thermal effect is excluded to be the cause of the failure in [9] whereas it is the basis of the simulation analysis in [10] to explain the failure mechanism. The SC behaviour of enhancement mode GaN Power HEMTs was experimentally studied for lower voltage (<200 V) devices [11] and with the help of finite element simulations for 650 V devices [12]. In both papers an extensive characterization of the SC behaviour of 650 V enhancement mode GaN Power HEMTs is missing.

The objective of this paper is to present the results of an experimental study about the behaviour of 650 V enhancement mode GaN Power HEMTs in SC. It is shown that the thermal increase is not enough to explain the failure of the devices under test [9]. Two failure mode are presented: one involving the local increase of the temperature, the other one more associated with instabilities exhibited by the devices. In addition, it is shown that high frequency oscillations appear on the gate and drain waveforms in particular test and circuit conditions. These oscillations indicate the presence of possible instabilities which the analyzed devices can suffer from.

2. Description of the experimental setup

Commercially available 7.5 A–650 V enhancement mode GaN on silicon Power HEMTs, produced by GaN Systems, were used as Devices Under Test (DUTs) [13]. They exhibit on state drain to source resistance, $R_{DS(on)} = 200\ m\Omega$ and gate threshold voltage, $V_{GS(th)} = 1.3$ V. The inspection of a delidded sample has shown that the die of $1.7 \times 2\ mm^2$ is mounted in a $5.01 \times 6.56\ mm^2$ surface mounting package. The active part of the device is made of several stripes with variable lengths and inter-source pitch of about 45 μm. From the literature [12] we can assume that a recessed p-doped GaN layer on top of an AlGaN/GaN heterostructure technology was used for the tested devices [14].

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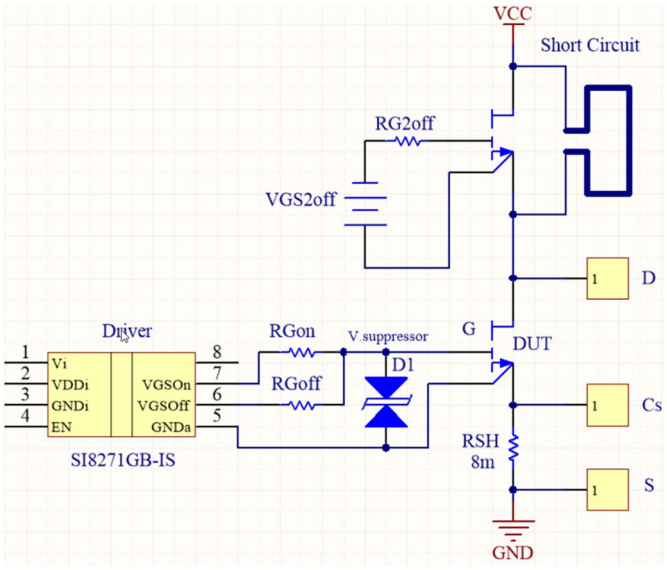

Fig. 1. Picture of the circuit used for the tests.

Schematic and picture of the experimental setup used to test the devices are reported in Figs. 1 and 2, respectively. The circuit consists of two GaN Power HEMTs connected in a single inverter leg configuration. The main parameters of the circuit are reported in Table 1. The Printed Circuit Board, PCB, was studied to minimize the stray inductance in both drain and gate branches in order to minimize inductive oscillations due to the very fast transient current variations. The stray inductance of the drain circuit was measured with a Vector Network Analyser to be lower than 3 nH. The total short circuit inductance L_{SC} becomes ~10 nH due to a short wire inserted in the circuit for measuring drain current with a Rogowski coil. The output current is also measured with a resistive shunt, $R_{SH} = 8\ m\Omega$ (see Fig. 1), made of four parallel resistors between the source and the ground. A voltage suppressor is placed between gate and ground to prevent damages to the external instruments in case of DUT failure. A negative voltage is applied to the gate during the device turn-off to avoid possible undesired turn-on due to gate voltage oscillations.

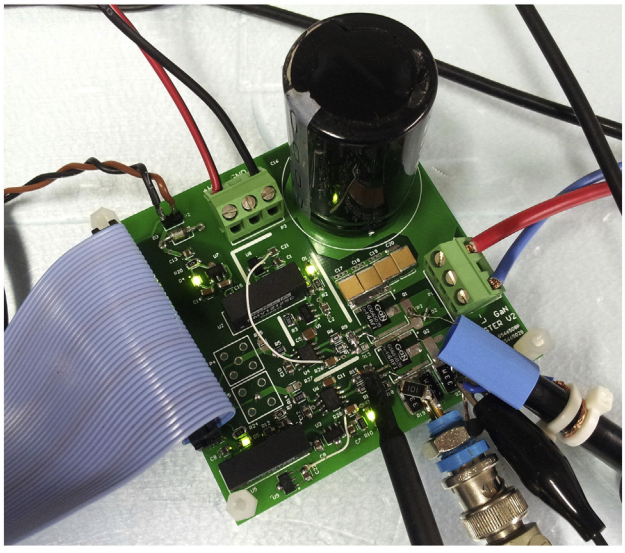

Fig. 2. Schematic of the circuit used for the tests.

In all the tests, DUTs were always mounted in the low side of the inverter leg whereas the high side device was always kept in the off state with −3 V at its gate.

3. Experimental results and discussion

The executed tests have shown two kinds of behaviors: a) the failure of the DUTs happens after several tens of microseconds and involve large energy; b) the failure of the DUT is registered after few hundreds of nanoseconds and involve a much smaller amount of energy.

Main results are summarized in the following subsections.

3.1. Short circuit with high failure energy

The typical waveforms of drain and gate voltages and currents during a destructive SC are reported in Fig.3 (a) and (b), respectively. The test conditions are: $V_{DS} = 300$ V and $V_{GSon} = 5$ V. The waveforms have a shape similar to those reported in literature for analogous experiments [8,9,10]. The failure takes place after 308 μs after the short circuit start with an involved energy of about 220 mJ. It is worth to recognize that V_{GS} tends to decrease and I_G to increase before the failure as expected when the junction temperature significantly increases [9]. Moreover, we can observe high frequency oscillations appearing in the first part of the short circuit. Their occurrence will be discussed in subsection 3.3.

Several tests have been executed with different V_{DS} and V_{GSon}. A summary of the obtained results is shown in Fig. 4 which reports the time to failure as a function of the average power dissipated during the destructive SC phase, P_{av}, computed as:

$$P_{av} = \frac{1}{t_F - t_0} \int_{t_0}^{t_F} i_D v_{DS} dt \quad (1)$$

where: t_o is the time at which the SC starts, t_F is the time to failure, i_D and v_{DS} are the measured waveforms of drain current and drain to source voltage, respectively.

The results of Fig. 4 confirm that the failure is the consequence of the increase of the device temperature behind a thermal limit. To prove that we have estimated the temperature reached by the device immediately before the failure. For this purpose we have used the normalized transient junction to case thermal impedance, k_{Zth}, of the analyzed device reported in Fig. 5 [13]. The single pulse characteristic applies to our case. This characteristic can be approximated by the following equation:

$$k_{Zth} = 10^{(0.51 \cdot log_{10}\Delta t + 1.314)} \quad (2)$$

where Δt is the duration of the power pulse which is supposed to be rectangular. Eq. (2) is valid in the range 10^{-6} s–10^{-3} s (the red line in Fig. 5) which includes the times to failure of Fig. 4 comprised between 300 μs and 600 μs.

Table 1
Main symbols and parameters of the experimental setup.

Parameter description	Symbol	Value
DUT positive gate voltage	V_{GSon}	Variable
DUT negative gate voltage	V_{GSoff}	−3 V
DUT turn-on gate resistance	R_{Gon}	10 Ω
DUT turn-off gate resistance	R_{Goff}	10 Ω
Drain to source voltage	V_{DS}	Variable
Drain current	I_D	Variable
High side HEMT neg. gate voltage	V_{GS2off}	−3 V
High side HEMT gate off resistance	R_{G2off}	10 Ω
Short circuit stray inductance	L_{SC}	10 nH
Shunt resistor for I_D measure	R_{SH}	8.2 mΩ

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