Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Isothermal bending fatigue response of solder joints in high power semiconductor test structures

A. Betzwar Kotas, G. Khatibi *

Christian Doppler Laboratory for Lifetime and Reliability of Interfaces in Complex Multi-Material Electronics, Chemical Technologies and Analytics, TU Wien, Getreidemarkt 9/CT-164, 1060 Vienna, Austria

ARTICLE INFO

Article history:
Received 22 May 2017
Received in revised form 29 June 2017
Accepted 30 June 2017
Available online xxxx

Keywords:
High-Pb solders
Accelerated testing
Bending fatigue
Reliability

ABSTRACT

Fatigue and cyclic delamination behavior of PbSnAg solders which are typically used as die attach material in power semiconductors was investigated. Isothermal bending fatigue tests were performed by using multilayered model test structures consisting of Si chips soldered on ceramic substrates and failure probability curves were obtained up to 1e8 loading cycles. The fatigue experiments were conducted by using an ultrasonic fatigue testing machine equipped with a three point bending set-up at a constant testing temperature of 80 °C. Detailed failure analysis of the fatigued samples revealed a dependency of the failure mode on the chemical composition of the high-Pb soft solders. The main failure modes included interfacial delamination of the Si-chip from the die attach, degradation due to crack propagation in the solder layer and in some cases partial fracture of the chip. Finally the feasibility of high frequency mechanical fatigue testing for screening and evaluation of solder joints in multilayered electronic systems is discussed.

1. Introduction

Large area solder joints provide the electrical and mechanical connection between the die, the ceramic substrate and the base plate in high power semiconductor devices. Though since 2006 processing of Pb-containing solders in electronics has been restricted by the RoHS directive, in case of high melting temperature type solders (i.e. solders with >85 wt% Pb and T_m > 300 °C) reliable alternatives have not been established yet [1]. Thus high lead containing alloys with typical compositions of Pb90Sn10, PbSn2Ag2.5 or alike are still in use for die attach applications in high power semiconductors due to their excellent wetting properties, relative microstructural stability, high ductility and reasonable costs. Furthermore, since Pb-free solders with lower melting point (~220 °C) are commonly used for the connection of substrate to the base plate, die attach re-melting during the assembly of the modules would not occur by using high-Pb solders.

During the processing and subsequent operation stresses are built up in multilayered electronic devices due to thermal mismatch. In the long term, repeated thermo-mechanical cycles may lead to initiation and propagation of cracks in the weak sites of the devices resulting in fatigue failure. In semiconductor devices, wire bonds and soldered layers between the chip and the substrate and those between the substrate and the base plate are known as the most vulnerable sites [2–5]. In advanced power semiconductor devices with improved wire bonding technologies chip solder fatigue has been identified as a serious reliability concern [2,6–8].

Active or passive thermal cycling tests which simulate the operational thermo-mechanical loading conditions in an accelerated manner, are conducted for reliability assessment of the whole device. Destructive die shear and pull is used to determine the quality and adhesion strength of the chip/substrate connection. Non-destructive X-ray and ultra-sound scanning microscopy can be used for identification of possible voids or delamination in soldered areas [3–6]. Mechanical testing methods such as static or cyclic bending tests are more common for evaluation of printed circuit boards and package assemblies [9–11]. Three- and four-point-bending tests have been used to simulate the flexure of the PCB in handheld electronic applications caused by single or repeated key strokes. It has been reported that for lower deflection levels, the failures are dominated by mechanical fatigue of solder joints, while larger deflection levels cause board failure due to trace breaking and pad rip-off [10–12]. A large number of studies have been conducted to study the isothermal low cycle fatigue behavior of solder joints in shear and bending mode based on which lifetime prediction models have been established.

Mechanical fatigue testing at higher frequencies has been proposed as a time saving alternative for rapid screening and lifetime determination of a variety of interconnects in microelectronics [13]. Increasing the mechanical testing frequency allows a considerable reduction of the testing time. However the procedure is only meaningful if a failure mode similar to that induced during the operational conditions is evoked. Ultrasonic resonance testing systems with frequencies in the

* Corresponding author.
E-mail address: Golta.khatibi@tuwien.ac.at (G. Khatibi).

http://dx.doi.org/10.1016/j.microrel.2017.06.095
0026-2714/

range of 20 kHz are used for investigation of fatigue life of various materials [14] and interconnects [13] up to very high cycle regime. Ultrasonic bending fatigue testing has been proposed for investigation of crack growth behavior and flexural fatigue response of metals and different composite materials [14].

In this work the high cycle fatigue performance of two types of Ni/PbSnAg/Ni solder joints was studied. The test structured were especially prepared with a design similar to that used in commercial semiconductor devices. The objective was investigation of the feasibility of high frequency mechanical bending fatigue testing as a method for lifetime and reliability assessment of thin solder joints in multilayered electronic systems.

2. Experimental

2.1. Sample design

Commercial high power IGBT-chips with Ni back side metallization were soldered onto the Ni coated Cu surface of ceramic substrates by using two types of PbSnAg solder alloys with Pb > 85 wt% and different contents of Sn. In order to avoid cracking and fracture of the ceramic substrate during the three point bending test, a thin sheet of steel with a thickness of 750 μm was glued at the reverse side of the substrate. The thickness of solder layer was in the range of 90–140 μm and the overall dimensions of the sandwich test structures were 15 × 27 mm (Fig. 1).

The microstructure of the solder joints consisted of a Pb-reach solid solution with fine precipitates and larger particles of Ag_3Sn and β-Sn grains (Fig. 2a and b). This typical microstructure of Pb-reach PbSnAg alloys is formed due to the limited solubility of Sn and Ag in the Pb-rich matrix. The interfaces of the solder at the chip and substrate side consisted of thin shallow scallops of NiSn intermetallic compounds (IMC) with average thicknesses of about 0.7–0.9 μm next to which Ag_3Sn and β-Sn particles were occasionally found. Large agglomerates of Ag_3Sn were found within the solder joints with lower Sn content (Fig. 2a) while β-Sn grains were more abundant in the alloy with higher Sn content (Fig. 2b).

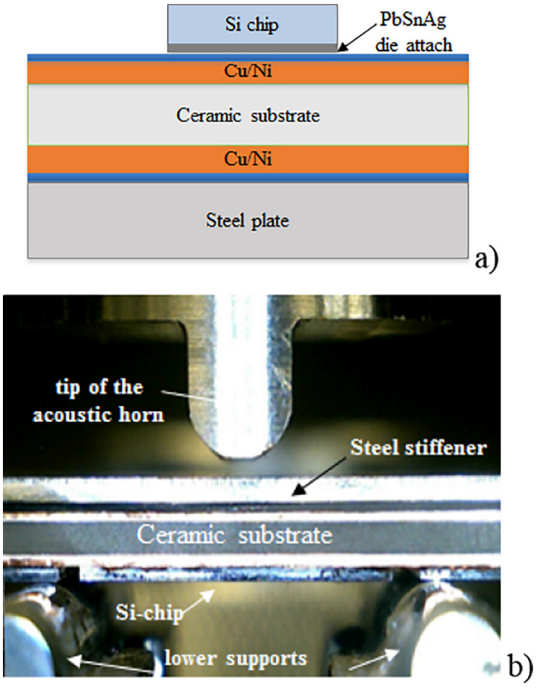

Fig. 1. Schematic cross-section of the multi-layered sample (a), image of the sample and the 3PB-stage, the steel plate is contacted to the acoustic horn and the chip is placed between the two supports (b).

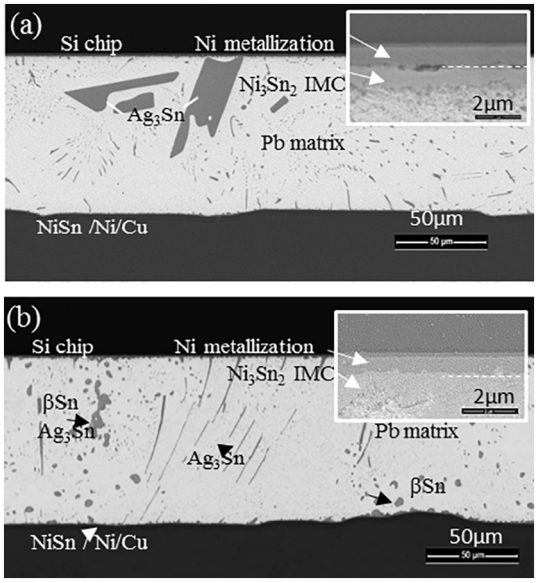

Fig. 2. Cross-sections of solder joints with inserts showing the magnified SEM images of the interfaces of Si-Ni/PbSnAg-1/Ni-Cu (a), and Si-Ni/PbSnAg-2/Ni-Cu (b).

In accordance with the PbSnNi ternary phase diagram, Ni_3Sn_4, Ni_3Sn_2 and Ni_3Sn intermetallics can be formed between PbSn solders and Ni substrates. The composition of the IMC layers is highly related to the Sn concentration in the solder, the reaction time and temperature and the substrate metallurgy [15,16]. According to the EDX analysis (Energy-dispersive X-ray spectroscopy) the composition of the NiSn phase at the chip side was found to be in the range of 58–62 wt% Sn and 38–42 wt% Ni indicating formation of Ni_3Sn_2 phase in both alloys. The inserts in Fig. 2a and b show details of the Ni-metallization and the IMC layers and with the dashed lines showing the interface between the both layers. Small voids (thin gap) were frequently formed in the Ni/IMC interface of the PbSnAg-1 (low-Sn), while the PbSnAg-2 joints displayed a well-defined closed interfacial line.

2.2. Resonance fatigue test set-up

Fatigue experiments were performed using an ultrasonic resonance testing system consisting of a power supply, a piezoelectric transducer, an acoustic horn equipped with a tip and the sample as schematically

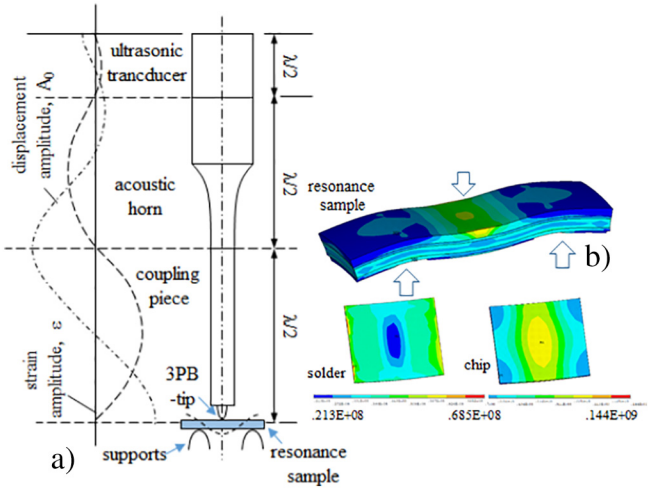

Fig. 3. Schematic image of the ultrasonic resonance fatigue testing system with three point bending set-up (a), stress distribution plots of the multilayered sample, solder layer and Si-chip (b) subjected to three point bending load.

Please cite this article as: A. Betzwar Kotas, G. Khatibi, Isothermal bending fatigue response of solder joints in high power semiconductor test structures, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.06.095