MR-12508; No of Pages 6

ARTICLE IN PRESS

[Microelectronics Reliability xxx \(2017\) xxx–xxx](http://dx.doi.org/10.1016/j.microrel.2017.06.091)

Contents lists available at [ScienceDirect](http://www.ScienceDirect.com/)

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Lifetime of power electronics interconnections in accelerated test conditions: High temperature storage and thermal cycling

Wissam Sabbah $^{\rm b}$, Faical Arabi $^{\rm a}$, Oriol Avino-Salvado $^{\rm b}$, Cyril Buttay $^{\rm b, *}$ $^{\rm b, *}$ $^{\rm b, *}$, Loïc Théolier $^{\rm a}$, Hervé Morel $^{\rm b}$

^a *University of Bordeaux, IMS Laboratory, UMR 5218, F-33405 Talence, France*

^b *Univ Lyon, INSA-Lyon, CNRS, Laboratoire Ampére, UMR 5005, F-69621 Lyon, France*

ARTICLE INFO

Article history: Received 21 May 2017 Received in revised form 14 June 2017 Accepted 30 June 2017 Available online xxxx

Keywords: Power electronics Wirebonding AuSn solder

ABSTRACT

We investigate the effect of three testing conditions (thermal shock, Rapid Temperature Change - RTC and high temperature storage) on the interconnects of a power electronic module. In particular, the mechanical strength of thick aluminium wirebonds is investigated and shows that while it is not affected by storage at 230 ◦C, it is much more sensitive to thermal cycling. Shock tests are found to be especially severe, despite having a smaller temperature swing than RTC. Regarding the die attach, no noticeable reduction in mechanical strength is found, regardless of the ageing conditions, and despite clear micro-structural evolutions.

© 2017 Elsevier Ltd. All rights reserved.

1. Introduction

In many applications, such as aerospace or automotive, power electronics systems are expected to operate over a wide ambient temperature range (more than 200 ◦C temperature swings, [\[1\]\)](#page--1-0). This is especially true for silicon-carbide (SiC) devices, as their maximum junction temperature is usually higher than that of their silicon counterparts.

Deep thermal cycling causes a high level of thermo-mechanical stresses in the packaging of these systems. Also, the high temperature encountered during the thermal cycle accelerates mechanisms such as the diffusion of chemical species at the interfaces, which in turn may cause weaknesses in the packaging.

As the reliability of power electronic modules was found to be unsatisfactory [\[2,3\],](#page--1-1) and as the thermal stresses are only expected to increase in the foreseeable future, there is a need to improve the current packaging technologies.

For example, regarding the die attach, many solutions are available, from Au or Zn-based solder to glasses or silver sintering [\[4,5\].](#page--1-2) Silver sintering is a promising technology, but it uses a very different process compared to soldering. Among solders, AuSn is an attractive lead-free replacement for High Melting Point (HMP) solders (which contain 95% lead). The melting point of AuSn is limited (281 ◦C), but

Corresponding author. *E-mail address:* [cyril.buttay@insa-lyon.fr](mailto: cyril.buttay@insa-lyon.fr) (C. Buttay).

<http://dx.doi.org/10.1016/j.microrel.2017.06.091> 0026-2714/© 2017 Elsevier Ltd. All rights reserved. it is easier to implement than more demanding alloys such as AuGe or AuSi [\[4\].](#page--1-2)

Regarding the ceramic substrates, $Si₃N₄$ has been identified as the most attractive material for reliable substrates [\[5,6\].](#page--1-3) Indeed, its flexural strength (700 MPa) is almost double of that of Al_2O_3 (450 MPa) or AlN (350 MPa) [\[7\].](#page--1-4) On the contrary, AlN is attractive for its high thermal conductivity.

Another weak point is the die topside interconnection, usually based on aluminium wirebonds. Aluminium is chosen because it is cheap (wires used in power electronics are much thicker than in microelectronics, 200-500 µm vs. 25-50 µm in diameter), it does not harden when cycled, and it is a good electrical conductor. There are, however, concerns regarding the reliability of the wires: the wire/die interface, in particular, generates thermo-mechanical stresses due to the mismatch in coefficient of thermal expansion (CTE) between a SiC die (\approx 4 ppm/K) and the aluminium wire (\approx 23 ppm/K). Thermal cycling tests listed in the literature range from 10 cycles between −196 and 500 ◦C [\[8\]](#page--1-5) to 12,000 cycles between 45 and 175 ◦C [\[9\].](#page--1-6) Another concern is the evolution of the micro-structure at the interface between the wire and the copper layers of the ceramic substrate. Usually, these copper layers receive a Ni/Au finish. Au is often mentioned as causing Kirkendall voiding with Al [\[5\].](#page--1-3) However, some experimental tests [\[10\]](#page--1-7) with Al wires bonded on NiAu-finished tracks only detected the occurrence of Al/Au Intermetallic Compound (IMC) after more than 7000 h at 250 ◦C.

In this paper, we focus on AuSn die attaches and aluminium wires. These interconnection technologies were selected for an aircraft application where reliability is the main concern. AuSn was

Please cite this article as: W. Sabbah et al., Lifetime of power electronics interconnections in accelerated test conditions: High temperature storage and thermal cycling, Microelectronics Reliability (2017), <http://dx.doi.org/10.1016/j.microrel.2017.06.091>

ARTICLE IN PRESS

2 *W. Sabbah et al. / Microelectronics Reliability xxx (2017) xxx–xxx*

chosen as a lead-free alternative to HMP solder alloys. The reliability of these interconnection technologies is evaluated in thermal cycling conditions as well as in high temperature storage (isothermal conditions). In the next section, we detail the test protocol. Then, in [Sections 3 and 4](#page--1-8) we present the results regarding the wirebonds and die attach respectively. Our conclusions are given in [Section 5.](#page--1-9)

2. Test protocol

2.1. Preparation of the test vehicles

The test vehicles used in this article were prepared by Microsemi, using silicon carbide diodes (also from Microsemi, 4.79×4.79 mm², 380μ m-thick with 5.7μ m Al as the top metal) and ceramic substrates sourced from two manufacturers:

- $Si₃N₄$, Active Metal Braze (AMB) substrates from the company Kyocera (referenced to as "K" in the remaining of the article), with a $320 \mu m$ -thick ceramic layer, $300 \mu m$ -thick copper on one side and 200 µm on the other side;
- AlN AMB substrates from the company Dowa (referenced to as "D"), with $300 \mu m$ -thick copper layers (both sides) and 635 µm-thick ceramic.

In both cases, the substrate pattern is identical (see [Fig. 1\)](#page-1-0), and a Ni/Au ENIG plating was applied by the manufacturer $(5 \mu m)$ Ni and 50 nm Au). The SiC dice are soldered onto the substrates using Au80Sn20 solder alloy (melting point 281 ◦C).

Each diode is connected using 8 aluminium wirebonds (diameter 254 μ m). In some cases (175 °C storage, described below), the test vehicles were split into 5 samples using a low speed diamond saw (Escil Labcut 150, with a Presi LM+ blade) to allow for more tests.

2.2. Accelerated test conditions

Two kinds of accelerated tests were performed:

- Storage tests (isothermal tests), in which the samples are exposed to a constant, elevated temperature over a long period of time. These tests are expected to trigger temperaturesensitive phenomena such as diffusion of chemical species.
- Temperature cycling tests, where the samples are exposed to large temperature swings. This generates thermo-mechanical stresses in the samples, which trigger fatigue mechanisms.

For the thermal cycling tests, two temperature profiles were chosen, to provide two largely different testing conditions:

• Rapid Temperature Change (RTC): −55 °C, maintained for 15 min, ramp-up at 10 $\mathrm{C/min}$ up to 175 °C, 15 min at 175 °C and ramp-down at 10 ◦C/min, in a Climats Excal 1423-TE chamber. Each cycle lasts for 76 min.

• Shock: $-40/+125$ °C temperature swing, in a two-chamber system (Climats CTr series) which generates very fast temperature changes (estimated at 65 ◦C/min). The samples are moved every 15 min.

Regarding the storage conditions, a preliminary test was performed: some test vehicles were submitted to a "step stress", during which the temperature was increased from 170 to 270 °C by 20 °C steps every 24 h. For each step, two samples were removed from the oven, and characterized (die shear test, wires pull and shear test, and microsections). No evolution could be detected from these mechanical tests [\(Fig. 2\)](#page--1-10). The micro-structure followed a classical evolution, with a coarsening of the phases, and the thickening of the interfacial intermetallical compounds of the solder joint, but no indication of advanced degradation was found. As the melting point of the AuSn alloy is 281 $°C$, it was decided to perform the ageing at a noticeably lower temperature: 230 ◦C. In parallel, a series of samples was stored at 175 ℃ to provide a comparison with the RTC cycling tests. For practical reasons, the 230 ◦C-storage tests were performed in a nitrogen atmosphere, while all the other tests (175 ◦C storage and all cycling tests) were performed in air. The composition of the atmosphere (air or nitrogen) was not found to have any particular consequence on the results.

D-type substrates failed early during the cycling tests (before the first 500 cycles for RTC and 2500 cycles for shock). This is not surprising, as AlN ceramic (used in D-type) is not as tough as $Si₃N₄$ (used in K-type) [\[11\].](#page--1-11) As a consequence, and because this article focuses on investigating the interconnections (die attach and wirebond), we only present cycling results for the K-type substrates. D-type and K-type results are presented for storage, as it induced no substrate failure.

2.3. Characterization

The tests and corresponding characterization were performed in two laboratories: Laboratoire Ampère (Lyon, France) for the storage tests, and IMS (Bordeaux, France), for the cycling tests. As a consequence, a special care was taken to ensure consistent results between both teams.

For each data point presented below, the samples were characterized as follows. At IMS, a sample with 5 dice was removed from the cycling chambers for mechanical testing, and a sample with two dice was taken for microsection. At Ampère, only one sample was used, with 4 dice used for mechanical tests, and one for microsection.

For mechanical characterization, a Dage 3000 was used at IMS, with the following parameters: for die shear, a 100 kgf load cell, a tool speed of 100 μ m/s, and a tool height of 70 μ m; for the wire pull, a 1 kgf load cell and a tool speed of $250 \mu m/s$. At Laboratoire Ampère, the test system was a XYZTEC Sigma Condor, with a 200 kgf load cell for die shear, a tool height of 80 µm, and a tool speed of $200 \mu m/s$; for wire pull, a tool speed of $600 \mu m/s$ and a 10 kgf load cell. At Ampère, pull tests were performed on half of the wires

Fig. 1. Photograph of the test vehicles. Two configurations were used (based on the same substrate, the dice being mounted on one side or the other): 5 dice or 2 dice.

Please cite this article as: W. Sabbah et al., Lifetime of power electronics interconnections in accelerated test conditions: High temperature storage and thermal cycling, Microelectronics Reliability (2017), <http://dx.doi.org/10.1016/j.microrel.2017.06.091>

Download English Version:

<https://daneshyari.com/en/article/4971643>

Download Persian Version:

<https://daneshyari.com/article/4971643>

[Daneshyari.com](https://daneshyari.com)