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Impact of the gate driver voltage on temperature sensitive electrical parameters for condition monitoring of SiC power MOSFETs

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ABSTRACT

Condition monitoring using temperature sensitive electrical parameters (TSEPs) is widely recognized as an enabler for health management of power modules. The on-state resistance/forward voltage of MOSFETs, IGBTs and diodes has already been identified as TSEPs by several researchers. However, for SiC MOSFETs, the temperature sensitivity of on-state voltage/resistance varies depending on the device and is generally not as high as in silicon devices. Recently the turn-on current switching rate has been identified as a TSEP in SiC MOSFETs, but its temperature sensitivity was shown to be significantly affected by the gate resistance. Hence, an important consideration regarding the use of TSEPs for health monitoring is how the gate driver can be used for improving the temperature sensitivity of determined electrical parameters and implementing more effective condition monitoring strategies. This paper characterizes the impact of the gate driver voltage on the temperature sensitivity of the on-state resistance and current switching rate of SiC power MOSFETs. It is shown that the temperature sensitivity of the switching rate in SiC MOSFETs increases if the devices are driven at lower gate voltages. It is also shown, that depending on the SiC MOSFET technology, reducing the gate drive voltage can increase the temperature sensitivity of the on-state resistance. Hence, using an intelligent gate driver with the capability of customizing occasional switching pulses for junction temperature sensing using TSEPs, it would be possible to implement condition monitoring more effectively for SiC power devices.

1. Introduction

The degradation of solder joints and wirebonds in traditional packaging systems usually results in an increase in the thermal resistance and hence, a higher junction temperature [1]. The use of temperature sensitive electrical parameters (TSEPs) for identifying the junction temperature of power semiconductors is one of the main techniques used for the implementation of condition monitoring strategies [2], which can be used for assessing ageing damage, improving the lifetime of the module and defining operational constraints. The use of TSEPs for condition monitoring has made the electrothermal characterization of power devices and modules essential for effective implementation.

Silicon carbide power devices have demonstrated a superior energy conversion efficiency due to the lower switching losses and on-state voltages. The wide bandgap of SiC (~3.3 eV) although beneficial for high temperature applications, nevertheless, makes condition monitoring using TSEPs more challenging since the electrical parameters are less temperature sensitive.

The turn-on current switching rate dI_{DS}/dt has previously been shown to increase with temperature and has thus been identified as a potential TSEP [3]. Due to the impact of parasitic inductance under high dI/dt conditions, the temperature sensitivity was shown to improve when the SiC MOSFET was driven at slower switching speeds. However, since the advantages of SiC are best exploited when driven at high switching speeds, the ability to sense the junction temperature using the switching rate, without increasing the switching losses is a critical challenge. Advanced intelligent gate drivers [4] would be a fundamental tool for implementing these techniques, where an advanced gate driver capable of momentarily implementing customized switching pulses as part of a condition monitoring strategy, would be a significant advantage. In this sense, a diagnostic pulse can be designed to maximize the temperature sensitivity of the current switching rate and/or on-state resistance of the device during the parameter evaluation and perform multiple measurements to minimize ambient noise.

This paper evaluates how the gate driver voltage (V_{GG}) of SiC MOSFETs can be used to maximize the temperature sensitivity of the on-state resistance $R_{DS\text{-}ON}$ and the switching rate of the drain current dI_{DS}/dt for more effective junction temperature sensing. The information generated here can be used for the development of condition monitoring strategies in SiC devices/modules in the future.

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2. Impact of gate driver voltage on temperature sensitivity of the on-state resistance

2.1. MOSFET on-state resistance analysis

The on-state resistance of a MOSFET device ($R_{DS\text{-}ON}$) is the resistance between the drain and the source of a MOSFET during conduction. This resistance is comprised mainly by 3 different components given by Eq. (1), as the current path within the MOSFET is formed by different layers [5].

$$R_{DS-ON} \sim R_{CH} + R_{JFET} + R_{DRIFT} \quad (1)$$

R_{CH} is the channel resistance which is inversely proportional to the carrier density within the channel as well as carrier mobility. Since the carrier density in the channel has a positive temperature coefficient due to the reduction of the threshold voltage with temperature and the effective mobility has a negative temperature coefficient, the temperature dependency of the channel resistance depends on the gate-source voltage V_{GS}. When V_{GS} is close to the threshold voltage (V_{TH}), then R_{CH} has a negative temperature coefficient, however, as V_{GS} increases and the channel becomes fully formed with carriers, the negative temperature coefficient of the effective mobility dominates hence, the temperature coefficient of R_{CH} becomes positive. The other two main resistive components, namely the JFET region resistance R_{JFET} (which is minimized for trench MOSFETs) and the drift region resistance R_{DRIFT}, have positive temperature coefficients. The gate voltage V_{GS} applied to turn-on the device affects the value of the resistance. This is a well-known fact and is one of the reasons why SiC MOSFETs require a high gate voltage in order to properly invert the channel and obtain a low on-state resistance compared with silicon MOSFETs [6,7], as well as avoiding a negative temperature coefficient, which can cause thermal runaway in case of paralleled devices.

In addition to the intrinsic device resistance modelled by Eq. (1), there are parasitic resistances which add to the total resistance of the packaged MOSFET chip. These include the wirebond resistances, metallization, solder, mounting substrate, etc., which will add to the total resistive path within the packaging, as shown in Fig. 1. It is important to mention that a recent packaging trend consists in the addition of a kelvin connection so as to minimize the impact of the stray inductances on the switching performances. The use of this additional terminal for evaluating bond-wire degradation and chip degradation has been demonstrated in [8] by characterizing the on-state voltage.

2.2. SiC MOSFET on-state resistance characterization

Fig. 2 shows the measured on-state resistance for a 1200 V/24 A SiC MOSFET with datasheet CMF10120D from Cree/Wolfspeed, at different V_{GS} voltages, ranging from 10.5 V to 20 V and temperatures of 22 °C and 125 °C.

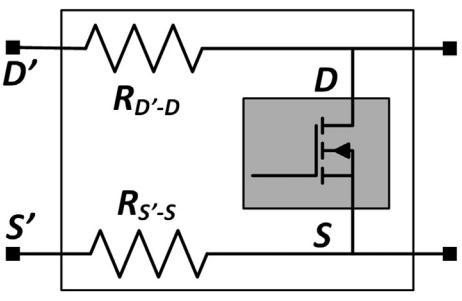

Fig. 1. Impact of stray resistances on the measured on-state resistance of a packaged MOSFET and kelvin connection.

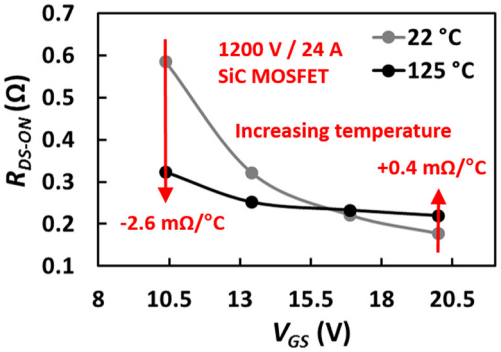

Fig. 2. Measured $R_{DS\text{-}ON}$ of a 1200 V/24 A SiC MOSFET as a function of V_{GS} for 22 °C and 125 °C.

The on-state resistance was measured at low currents by injecting a sensing current of 50 mA and measuring the on-state voltage with a digital multimeter Hameg HMC8012 while applying different gate voltages. The measurements were made using a basic test setup and the measured values agree with datasheets and literature. In Fig. 2, it can be seen that the temperature coefficient of $R_{DS\text{-}ON}$ is negative at low V_{GS} and becomes positive as V_{GS} increases. This characteristic is peculiar to high voltage SiC MOSFETs because the channel resistance is a considerable fraction of the total resistance unlike silicon MOSFETs where the total resistance is dominated by the voltage blocking drift region. This is because the resistance of the drift region in SiC is smaller since significantly thinner layers are required for blocking high voltages as a result of the higher critical electric field in SiC. The on-state resistance of a 1200 V/20 A Si MOSFET from IXYS, with datasheet number IXFX20N120P as a function of the gate voltage is shown in Fig. 3, for temperatures of 22 °C and 125 °C. It can be clearly observed how, for the voltage range selected, there is no impact of the gate voltage on the on-state resistance. However, the temperature sensitivity is considerably higher with +6.4 mΩ/°C. In the case of the SiC MOSFET, the temperature sensitivities for a gate voltage of 20 V and 10.5 V are +0.4 mΩ/°C and −2.6 mΩ/°C respectively.

Recently, after the emergence of SiC Trench MOSFET devices, it seems to be the technology adopted by different manufacturers. Trench MOSFETs have a lower input capacitance and a lower on-state resistance for the same device area compared with a planar MOSFET. This reduction of the on-state resistance appears as a result of the reduced channel resistance together with the elimination of the JFET region of the MOSFET [5,9], as can be seen from Eq. (1).

The on-state resistance of a 650 V/39 A trench SiC MOSFET from Rohm, with datasheet reference SCT3060AL is shown in Fig. 4, where the on-state resistance as a function of temperature has been characterized for gate voltages of 20 V and 10.5 V. The temperature sensitivities are +0.14 mΩ/°C and −1.0 mΩ/°C respectively.

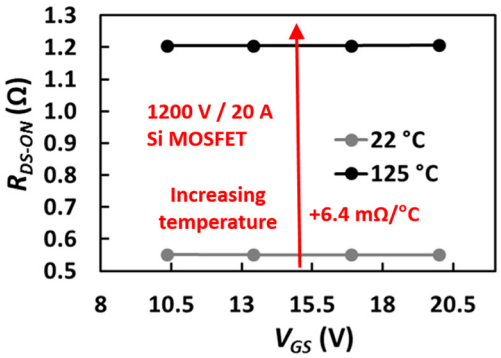

Fig. 3. Measured $R_{DS\text{-}ON}$ of a 1200 V/20 A Si MOSFET as a function of V_{GS} for 22 °C and 125 °C.

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