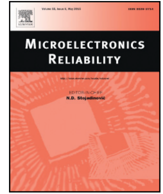
Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Impact of load pulse duration on power cycling lifetime of chip interconnection solder joints

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A R T I C L E I N F O

Article history:
Received 19 May 2017
Received in revised form 29 June 2017
Accepted 29 June 2017
Available online xxxx

Keywords:
Power electronics
Reliability
Power cycling test
Empirical lifetime model
Failure mechanisms

A B S T R A C T

Thermo-mechanical stress limits the useful life of power modules in the application. Active power cycling tests have been applied for more than three decades to investigate the degradation generated by thermo-mechanical stress in accelerated testing. Different lifetime models were proposed to extrapolate the lifetime from accelerated test results to application conditions. However, these lifetime models did not differentiate between the prominent failure mechanisms of Al wire bond degradation and solder fatigue in classical modules. By combining new, highly reliable interconnection technologies with classical technologies, those failure mechanisms can be investigated separately. In previous publications this concept of separation of failure modes was applied to study the impact of temperature swing and medium temperature on each failure mode in power cycling. In the present study, the impact of power pulse duration on the lifetime of chip solder and Al wire bonds is investigated. The results are another jigsaw piece for the goal of proposing a lifetime model for chip solder interconnections. The empirical data base is furthermore indispensable for the scaling and validation of physic-of-failure approaches in the process of lifetime modelling.

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1. Introduction

Due to varying power losses dissipated in the semiconductor switches, power electronic modules are subjected to thermal stress during operation. The temperature gradient in the layer system of the module in combination with the different coefficients of thermal expansion of the materials result in mechanical stress which generates degradation of the interconnection layers. This limits lifetime of power electronic modules in application.

For a reasonable designed power electronic system, electrical engineers need to know the lifetime of each component. By analysing typical mission profiles of an application, which represent the stress on a system and its components, engineers can estimate lifetime adequately if suitable lifetime models are available. The lifetime of power modules under thermo-mechanical stress have been investigated intensively in the past decades by accelerated DC power cycling test. The lifetime models derived from these studies have a pure empirical nature and are scaled upon a large database of power cycling test results. The first comprehensive lifetime investigation with numerous power cycling tests, which were conducted within the frame of the LESIT project in the early 90s [1], revealed the dependence of the lifetime not only on the temperature swing ΔT_j, but also on the medium junction temperature T_{jm}. In 2008 the CIPS lifetime model was presented [2]. Besides the influence of further operational factors, like the dependency on the load pulse duration t_{on} and the current density in the wire bond stitch, technological characteristics like the voltage class, representing the chip thickness, and the wire bond diameter were also taken into account.

However these lifetime models have in common that they do not distinguish between the failure mechanisms which occur in classical power electronic modules under thermo-mechanical stress. These are the degradation of the wire bond interconnection on the topside of the chip, and the solder fatigue of the chip interface to the DBC or of the DBC-baseplate connection. Due to the different thermo-mechanical behaviour of the involved materials and the different nature of the failure mechanisms these failures reveal individual dependencies on the load characteristics. Thus the lifetime limiting failure mechanism in an accelerated test might differ from the lifetime limiting failure mechanism at divergent load conditions. As a consequence the extrapolation of a dependency based on the test results without knowledge of the dominant failure mechanism might lead to wrong lifetime expectations in applications.

Today, new highly reliable connection technologies like aluminum-cladded copper wires for the topside [3], or the sinter technology for the chip connection to the DBC [4], allow the isolated investigation of the different failure mechanisms by combining a high reliable technology on the one side with a classical technology on the other side. This method of separation of failure modes [5] was used for the investigation

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http://dx.doi.org/10.1016/j.microrel.2017.06.081
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Please cite this article as: M. Junghaenel, U. Scheuermann, Impact of load pulse duration on power cycling lifetime of chip interconnection solder joints, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.06.081

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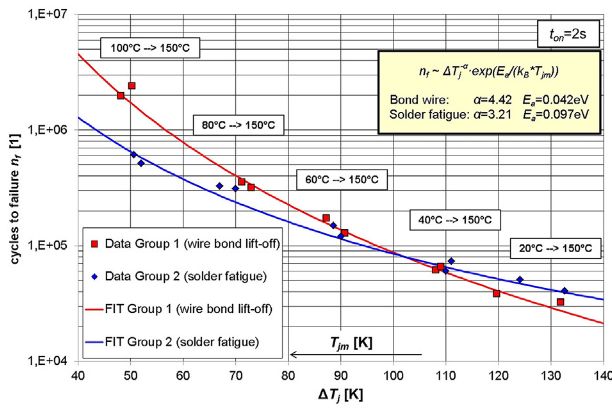

Fig. 1. PC-results of isolated failure mechanisms of classical modules in dependence on temperature swing ΔT_j [7].

of the influence of the temperature, i.e. the medium temperature T_{jm} in [6,7] and the temperature swing ΔT_j in [7]. The relation between temperature and lifetime limiting failure mode is illustrated in Fig. 1. Now, an investigation on the impact of the load pulse duration t_{on} on lifetime was conducted and the results are presented in the following. In the course of mission profile analysis the varying thermal stress is reduced to a number of simple stress reversals by appropriate counting methods, like the rainflow counting algorithm [8]. Hereby long term temperature variations as well as superimposed short term temperature cycles are considered.

On that account the load pulse duration was largely varied by three orders of magnitude in the present study. This ensures to capture the influence of pulse durations on lifetime more precisely.

2. Experimental approach

2.1. Test vehicles

In accordance to the previous investigations in [6,7] DC power cycling tests were performed on two groups of modules by switching a DC load current cyclically on and off.

The first group of modules consists of standard and commercially available SKiM63 modules [4]. This module comes in a six-pack configuration comprising three individual phase legs on separated power DBC substrates. Each switch consists of four 1200 V IGBT chips in parallel with a nominal chip current of 75 A each, such that the module has a nominal current rating of 300 A. The SKiM63 is a module without baseplate and is assembled in pressure contact technology. This means that the DBC substrate is directly pressed to the heatsink with a thermal paste interface when mounted. The inside connection technology is characterized by sintered chips and the topside chip connection is realized by aluminum wire bonds. Since the load current terminals are implemented by the pressure contacts and the auxiliary contacts by the spring technology the standard SKiM63 is a 100% solder-free module.

For the test vehicles of the second group the SKiM63 module was specially modified: The chips were not sintered but soldered to the DBC, while the topside connection of the chip is realized by aluminum cladded copper wires [3], which exhibit a much higher reliability than standard aluminum bonds. By this approach a separation of failure modes is achieved, since no degradation of the sinter layer is expected for group 1 and only bond lift-off will occur, while the solder fatigue will be the lifetime limiting failure mechanism for group 2.

2.2. Test conditions

A series of tests was defined with a large variation of the load pulse duration t_{on} from 0.07 s to 60 s. All tests were performed with modules of both groups simultaneously. The T_{jmax} was hereby set to $T_{jmax} = 150$ °C for all tests. The temperature swing ΔT_j was adjusted to $\Delta T_j = 110$ K for long load pulses of $t_{on} \geq 2$ s in order to shorten the test time, while for shorter load pulses $t_{on} \leq 2$ s the temperature swing had to be adjusted to $\Delta T_j = 70$ K since a temperature swing of $\Delta T_j = 110$ K would have required a load current that exceeds the maximum current rating of the module. The load current was adjusted in dependence of the load pulse duration t_{on} at the beginning of each power cycle test in order to set the desired temperature swing and ranged between 240 A and 425 A. The voltage V_{GE} was used for fine tuning of the temperatures and ranged between 12 V and 17 V. The modules were permanently cooled by water cooling. Cooling temperature was adjusted to set the medium temperature level of the test. As a result of the used test bench, which consists of two branches and which cycles the modules in each branch alternately, the cooling time t_{off} is automatically the adjusted load pulse duration t_{on}. Load and cooling settings where not changed during the whole power cycling test, so that degradation mechanisms had direct impact on the electrical and thermal behaviour of the module.

Junction temperatures were measured by the $V_{CE}(T)$-method that determines the virtual junction temperature which is actually equivalent to the area-related mean temperature of a chip, or in the present case of the paralleled chips, as described in [9].

Table 1
Power cycling test results in cycles of modules of group 1 and group 2 in dependence on load pulse duration t_{on}.

ΔT_j	t_{on}	$N_{f,\ Group\ 1}$	$N_{f,\ Group\ 2}$
70K	0.07 s	$5.27 \cdot 10^6$	$1.67/2.80 \cdot 10^6$
	0.1 s	$3.11 \cdot 10^6$	$2.27 \cdot 10^6$
	0.2 s	$1.48 \cdot 10^6$	$1.08/1.44 \cdot 10^6$
	1 s	$7.94 \cdot 10^5$	$4.12/4.41 \cdot 10^5$
	2 s	$3.27/3.59 \cdot 10^5$	$3.27/3.59 \cdot 10^5$
110K	2 s	$6.71/6.80 \cdot 10^4$	$6.40/7.90 \cdot 10^4$
	7 s	-	$5.10/5.10 \cdot 10^4$
	10 s	$4.67 \cdot 10^4$	$4.67/5.12 \cdot 10^4$
	30 s	$3.09 \cdot 10^4$	$4.46 \cdot 10^4$
	60 s	$2.77/2.77\ 10^4$	$3.65 \cdot 10^4$

3. Test results

All tests were conducted until end of life. Absolute lifetime in cycles is listed in Table 1. Since the investigation focused on the solder joint, testing for modules of group 1 was interrupted as soon as one switch of the half-bridge failed if the simultaneously tested module of group 2 had already failed completely. Fig. 2a illustrates the results of the presented test series with $\Delta T_j = 70$ K for $t_{on} \leq 2$ s and Fig. 2b plots the results of the test series with $\Delta T_j = 110$ K for $t_{on} \leq 2$ s.

The results for the failure mode of bond lift-off in the standard SKiM63 modules of group 1 are depicted by the red squares. As a reference the SKiM63 lifetime model [10] is given as a solid green line for a failure probability of 50%. For short load pulses the experimental results are in good agreement with the prediction by the SKiM63 lifetime model. For long pulses however the experimental results exhibit a decrease in lifetime with increasing load pulse duration, while the SKiM63 lifetime model assumes a rapid stagnation of the lifetime decline.

The test results of the soldered modules of group 2 are depicted in blue diamonds. In the range of short load pulses a lower gain in lifetime is perceptible for the solder connection than for the connection by wire

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