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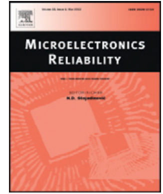

Determination of safe reliability region over temperature and current density for through wafer vias

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ABSTRACT

Circular and slot backside vias are stressed over current and temperature and the resulting failure times are fitted to Black's equation. Contour plots of the FIT rate are generated and the reliability of circular and slot vias are compared. It is demonstrated that in most cases the FIT rate of the circular via is statistically significantly lower than that of the slot via. However, both types are easily able to meet a goal of 100 FITs in 10 years at $T = 125$ °C and $J = 0.25 \times 10^6$ A/cm^2. The contour map of the FIT rate defines the region where the via can operate reliably. By use of the 95% upper confidence bound, the region of safe operation is reduced in size, adding a layer of margin to the prediction of via reliability. The approach described here provides a "reliability map" for designers allowing trade-offs between temperature current to be made when designing for high reliability.

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1. Introduction

GaAs die used in RF/microwave components are typically either wire bonded and or used in flip-chip assemblies. Through-wafer or backside vias (BSV) are often employed with Au or Cu back metal in a wire-bond assembly and less often in flip-chip designs where Cu pillar or solder bumps are more common. The via in a wire-bond assembly can act as both a ground node and/or thermal path to the bottom of the die for heat dissipation within the back metal and the connecting laminate epoxy. For cost-sensitive applications like consumer mobile wireless, GaAs die cost is critical. One method of lowering die cost is reducing the die size. A typical GaAs heterojunction bipolar transistor (HBT) wire-bonded power amplifier (PA) die has 6 to 8 through-wafer vias. BSV size reduction for a ~1 mm by ~1 mm GaAs HBT die can bring up to ~15% savings in die area [1]. However, reducing the BSV size and/or changing its shape brings reliability concerns because of the large currents they must handle.

The current carrying capability for a through-wafer via is important in the design of reliable and rugged circuits, especially as die size reduction is continually pushed. Often, the BSV current carrying capability has been assumed to be limited by the top-side metals feeding into it (not so much a rule as a guideline). This assumption is still made by a number of both GaAs and silicon foundries. Unfortunately, this belief has seldom been checked and designs have become overly aggressive. We surveyed our own parts and performed competitive analysis on others' components and found BSV current densities ranging from 54–850 mA/via for 50 μm diameter vias and from 92–700 mA/via for slot vias. From [2], we estimated that a slot via uses >500 mA. Thus, quantifying the current handling capability of our BSV is essential.

2. Choice of failure criterion

To assess the impact of a change in via resistance on performance, the effect of a resistance change on the operation of a power amplifier circuit was evaluated. Simulations were performed on both a load-pull structure and a full power amplifier circuit. The change in the gain of the amplifier due to an increase in via resistance was computed.

For a 4-cell load-pull structure, the resistance in the emitter path was expected to be dominated by the device emitter resistance + feed resistance. The via resistance would need to approach ~200 mohm before the gain would be noticeably reduced. In simulation, the BSV resistance of the load-pull structure had to be increased from 5 to 200 mohm before a 1 dB degradation in the RF gain was observed.

Also, simulations were performed on an entire power amplifier circuit where the resistance for all BSVs was increased to 1.3× the nominal value. The simulations showed virtually no change in the performance (S21) up to this value. In fact, the BSV resistance would need to increase by a factor of 30 (2900% increase) to change the gain by 1 dB for this particular circuit.

These two simulations indicate that any criterion <30× change in BSV resistance can be used as an accelerated test failure criterion.

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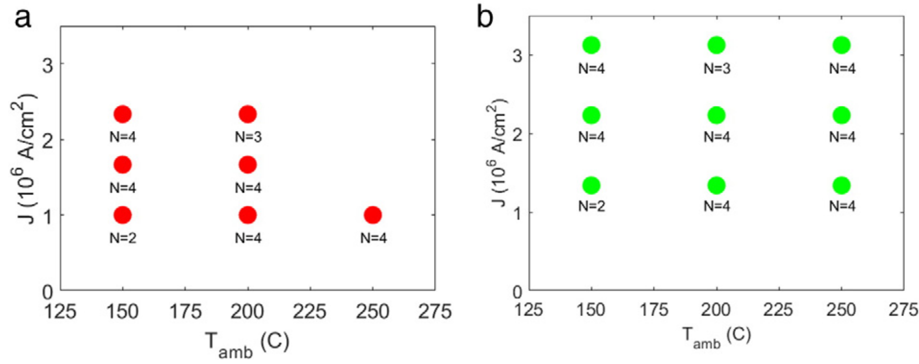

Fig. 1. a. Plot of experimental stress conditions for circular vias with their associated sample sizes. b. Plot of experimental stress conditions for slot vias with their associated sample sizes.

3. Experimental

A total of 58 test structures were stressed over a matrix of temperature (150–250 °C) and currents (3–7 A). Of the 58 BSV structures, 25 were 50 μm diameter circular controls and 33 were 20 × 40 μm rectangular slot vias. Originally, 33 circular vias were tested but 8 higher stress failures had to be excluded in order to eliminate a significant interaction between temperature and current density (see next section). All controls came from the same 2 wafer lot whereas the slot via structures were from a mix of 13 wafers from 3 different wafer lots. The stress conditions and sample sizes at each condition for each via type are shown in Fig. 1a and b.

The layout of the test structure for the circular via is shown in Fig. 2.[1] While the plan view area of the circular via was ~2000 μm^2, the area of the entire bond pad was ~1.4E6 μm^2. The front-side metal at the top of the via consisted of a predominantly gold evaporated stack with a total thickness of ~3 μm. The via metal was Cu and plated from the back-side. Schematic diagrams for circular and slot vias are shown in Fig. 3a and b. The thickness varied along the length of the via and had a minimum thickness of ~2 μm (see Figs. 5 and 6 also). Therefore, the pertinent cross-sectional area subjected to current stress was defined by the via circumference/perimeter where the thickness was a minimum. For the circular via, the minimum cross-sectional area was ~300 μm^2 and for the slot via, the corresponding cross-sectional area was ~224 μm^2. Since the lowest current used in this work was 3 A, the corresponding minimum current density was ~1E6 A/cm^2 for the circular via and ~1.3E6 A/cm^2 for the slot via.

Parts were stressed in 2 different test units or kits. The die containing the via test structure was mounted in a Stratedge 360 package using silver epoxy (EPOTEK 1011). Seven 5 mil Al bond wires were bonded to the package from the structure on the input side. The current density in the Al wires was ~8 kA/cm^2, much lower than experienced by the test structure and also much lower than the maximum allowable current density for these wires. Each package was bolted onto a heat source in each test kit. The heat source also acted as a large heat sink such that the self-heating of the via could be assumed to be zero.

The resistance of each via was monitored independently during stress and recorded every minute. Failure was defined to occur when the via resistance increased by 200% of its initial value (3× increase). Fig. 4 shows a typical plot of resistance vs. time for a failed via. Parts were stressed up to ~4200 h and most parts failed.

4. Statistical analysis

Failure times were fitted to Black's equation [3], given by

$$\ln(t_f) = lnA + \frac{E_a}{kT} + n * lnJ \tag{1}$$

where t_f is the failure time, E_a is the activation energy, T is the via temperature, n is the current density exponent, J is current density, A is a constant and k is Boltzmann's constant. A chi-square goodness of fit test was performed [4], comparing the fit of the failure times to the Weibull and lognormal distributions. For both via types, the lognormal was found to provide a better fit than the Weibull but the difference was not statistically significant. Historically, the lognormal has been favored for GaAs vias and so the failure distribution was assumed to be lognormal. The results of the fit to the above equation for slot and circular vias are given in Table 1.

To determine any difference between test kits, (1) was modified to

$$\ln(t_f) = lnA + \frac{E_a}{kT} + n * lnJ + B * kit \tag{2}$$

where B is an indicator variable which takes on a value of 0 for kit 1 and 1 for kit 2. For both slot and circular vias, the estimate of B was not significantly different than zero and so the effect of kit can be ignored.

The possibility of an interaction between temperature and current was also considered. Eq. (3) shows a modified version of (1) where an interaction term has been added.

$$\ln(t_f) = lnA + \frac{E_a}{kT} + n * lnJ + C * \frac{lnJ}{kT} \tag{3}$$

The coefficient C was estimated for both via types and was found to be statistically insignificant in both cases.[2] The lack of interaction is important for extrapolation since an interaction implies physically non-intuitive behavior. For example, a significant interaction between temperature and current indicates that there exists some temperature where an increase in current would *increase* lifetime. Similarly, a fixed current would then exist where an increase in temperature would *increase* lifetime. Since there was no significant interaction, (1) is adequate for making predictions.

The expected value of (1) is the log mean for the lognormal distribution, μ, where the median time to failure (MTTF) is exp.(μ). The cumulative distribution function (cdf) denoted by F is given by

$$F(t) = \Phi\left(\frac{\ln(t) - \mu}{\sigma}\right) \tag{4}$$

where t is time, Φ is the standard normal cumulative distribution function and σ is the lognormal shape factor.

[1] For the slot via, the figure would be similar but the red circle would be replaced by a rectangular slot.

[2] Four circular via parts at 250 °C and 7 A and four more at 250 °C and 5 A were excluded from the analysis in order to eliminate a significant interaction between temperature and current.

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