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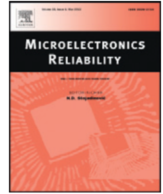

Evaluation of the impact of the physical dimensions and material of the semiconductor chip on the reliability of Sn3.5Ag solder interconnect in power electronic module: A finite element analysis perspective

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ABSTRACT

This paper primarily focuses on an evaluation study for the temperature cycling capability of tin silver solder interconnect in power electronic applications by the impact of die dimensions and die material properties. The study was investigated on finite element analysis perspective on chip/solder/substrate structure. A commercially available chip was chosen in the finite element analysis (FEA) as the nominal base die. Two thermal cycle profiles were utilised. The effect of die area, die thickness and material properties (Si and SiC) on the thermal cycling capability of the solder layer was investigated from FEA perspective. From the FEA, it was concluded that decrease in die thickness resulting in increment of thermal cycling capability of solder layer for both material (Si and SiC). Increase in die area increases the thermal cycling capability of solder. For higher ΔT thermal cycle, solder under SiC die perform better than solder under Si die in terms of thermal cycling capability. When the die thickness become smaller than a threshold value of the thermal cycle regime, solder under Si die have better thermal cycling capability than solder under SiC die. Additionally a parametric study was undertaken for a SiC chip/substrate structure under high ΔT temperature cycling profile for solder layer geometric parameter (wetting angle, titling angle and thickness). From the parametric study which utilised design of experiments (DoE), a wavelet radial basis surrogate model was generated. A sensitivity analysis was performed on surrogate model in order to identify the most influencing parameter. From the sensitivity analysis, it was concluded that wetting angle and solder layer thickness of solder layer have significant impact on the thermal cycling capability of the solder layer.
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1. Introduction

Power electronic module (PEM) devices are often exposed to rather harsh operating conditions, these devices consist of different material layers, and each material has different coefficients of thermal expansion (CTE), which induce thermo-mechanical stresses in each layers under its operating conditions. Many failure mechanisms in PEM devices were widely reported in the literature [1]. In a power electronic module, the silicon chip is attached by die attach materials usually solder materials to package substrate material. Temperature fluctuations in the power electronic module device during its service time causes gradual increase of damage in solder joints and eventually this damage accumulation passed beyond a critical value will lead to electrical failure of the PEM device. The package substrate is typically composed of ceramic isolated by copper layers. Silicon chips are gradually replaced by silicon carbide chips which can able to withstand a temperature up to 500 °C [1]. However die attach materials such as solders can't endure a temperature of above 200 °C. Lead free solders such as SnAg has the melting temperature of 221 °C. These lead free solders can be used as die attach material for up to 80% of the melting temperature before creep strain effects cause failure in solders [2].

One of the objectives of thermo-mechanical analysis is to generate a stress versus strain responses in solder layer and predict its reliability for a specified operating condition. An accurate reliability estimation of solder joints depends on accurate modelling of the mechanical and microstructure characteristics of the particular solder layer. The solder layer is mechanically soft and often used in high homologous temperature; hence, the plasticity and creep causes mechanical deformations in solder layer. Creep is the redistribution of stresses and strain with time in solder under a constant load at elevated temperature. Creep damage of solder joint is a process of formation and growth of voids and cavities within the solder microstructure, become significant above a homologous temperature of 0.4 [3]. Homologous temperature is defined as T/T_m, where T_m is the melting temperature. Often the solder layer in power module applications are very thin and bonded to relatively rigid materials such as copper and silicon with intermetallic layer formed at the bonding interfaces often display brittle characteristics.

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Nomenclature

$\Delta\varepsilon_{in}$	Accumulated equivalent inelastic strain during a stabilised cycle
V_j	Volume of one jth element
V_{tot}	Summation of volumes of all the elements within the volume
N_f	Fatigue life
α_i	Coefficient of thermal expansion of material *i*
ν_i	Poisson ratio of material *i*
E_i	Young's modulus of material *i*
h_i	Thickness of material *i*
ΔT	Temperature change
L	Half the length of the chip
G_i	Shear modulus of material *i*
τ	Interfacial shear stress
γ	Interfacial shear strain
D_i	Flexural rigidity of material *i*
k, κ, λ, ξ	Characteristic constants

Power electronic devices for switching applications based on wide band gap materials such SiC and GaN offer better performance on operating voltage, switching speed and on resistance compared to Si material [4,5]. This is due to wide gap material's higher breakdown electric field and higher thermal conductivity. Other significant device level advantages of SiC power devices compared to Si based power devices were listed on the book by Bai et al. [6]. A study by Herold et al. [7] on the power cycling capability of SiC diodes and Si diode for identical testing conditions was conducted. The study concluded that reliability of standard soldered SiC diode was three to four times lower in comparison with Si diode of similar rated current and voltage category. The influence of chip dimensions and material property on the thermal cycling capability of the Sn3.5Ag solder from finite element analysis perspective has not been analysed in the past

The motivation for this study arisen from the question of what is the trend to the thermal cycling lifetime capability of the solder layer

- If the chip thickness varies from a nominal base value such as $\times 0.333$, $\times 0.666$, and $\times 1.333$
- If the chip area varies from a nominal base value such as $\times 0.125$, $\times 0.25$, $\times 0.5$, and $\times 2$
- What is the difference between thermal cycling capabilities of solder layer under die if the die material properties change (Si instead of SiC)?

That motivated to conduct passive thermal cycling of structure for chips with various materials (Si and SiC) and dimensions in order to investigate the thermal cycling capability of solder influenced by thermally induced stresses. Additionally how the wetting angle, layer thickness, and tilting angle influences the thermal performance of the solder layer was also investigated by utilising a surrogate modelling approach combined with sensitivity analysis.

2. Finite element analysis of solder interconnect in power module

In order to evaluate the impact of die thickness, area and material properties on the thermal cycling capabilities of Sn3.5Ag, a CREE manufactured Schotkky diode chip (CPW5-1200-2050B) [8] was chosen as a base chip. The length, width and thickness of the base die are respectively 4.9 mm, 4.9 mm, and 380 μm. The standard substrate thickness of the structure are extracted from Lutz et al. [9]. Thickness of copper aluminium oxide, and solder are respectively 0.3 mm, 1 mm, and 0.1 mm. The wetting angle of the solder was chosen as 33° based on national institute of standard (NIST) report [10].

The length and width of the substrate for all the simulation were chosen as 20.4 mm. The elastic and thermal material properties of the materials used in this model were extracted from public domain [11] and the temperature depended solder material properties are from Kim's thesis [12]. The material properties used in the numerical modelling are listed in Table 1. Top and bottom metallisation on the chip was ignored in the finite element modelling since they contribute very little in terms of stresses and inclusion of the metallisation in the finite element analysis will increase the complexity of the modelling and the solution process. To simulate the thermo mechanical loading condition on a soldered structure in Ansys FEA software [13] we generated the three dimensional finite element model as shown in Fig. 1.

The Anand's viscoplastic model used in this study, was originally developed for high-temperature metal forming processes such as rolling, but it has been demonstrated for use in predicting the life of solder joints in electronic packaging. The Anand viscoplastic material properties of the solder layer were extracted from Wang's article [14] and [15] and they are listed in Table 2. The parts in the model associated with critical regions of interest have finer mesh in order to ensure accurate FEA results. In this study, FEA simulation in Ansys is a passive thermo mechanical analysis using the element SOLID185.

JEDEC standard [16] for temperature cycling is specifically for the solder interconnection testing on thermal chambers. Many studies on eutectic solder have shown that the dwell time beyond certain limit has a minimal effect on the Mean Time to Failure (MTTF). Additional dwell time will not produce additional damage beyond a limit or boundary. The faster ramp rate does impose more damage on solder joint than a slow ramp rate. According to Fan et al. [17], it was concluded that the ramp time and dwell time have conflicting effects on solder joint reliability and the finite element results were also shown that the majority of damage occurs during the ramp period.

As stated by Zhai et al. [18], the dwell time at high temperature is predicted to have a negligible contribution to the total inelastic strain energy density. Hence in this analysis ramp time and dwell time were taken as 3 and 15 min respectively based on the study by [18]. Maximum and minimum temperature sets are taken as [−25 °C, 50 °C], [−25 °C, 150 °C] for two ΔT regime. The structural boundary condition is as the three point freedom restraining boundary condition was imposed on the model.

Fig. 2 is the FEA output for plastic strain on the thin layer (10 μm) of solder. In order to evalaute the MTTF of the solder layer, tradionally a predictive fatigue life model was utlised. The predictive fatigue life time models can be categorised based on stress, plastic strain, plastic

Table 1
Elastic and thermal material properties used in the FEA.

Properties	Copper (Cu)	Aluminium oxide (Al_2O_3)	Silicon (Si)	Silicon carbide (SiC)	Solder (Sn3.5Ag)
Density (kg/cm^3)	8900	3985	2300	3210	7360
Coefficient of Thermal Expansion (10^{-6}/K)	16.9	5.8	3	4.3	21.
Young's modulus (GPa)	117	380	162	501	
52,708 − 61.74 ∗ T − 0.0587 ∗ T^2					
Poisson ratio	0.31	0.23	0.3	0.14	0.4

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