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Semiconductor package qualification based on the swelling temperature

K.H. Song *, J.S. Jang

Department of Industrial Engineering, Ajou University, 206, World cup-ro Yeongtong-gu, Suwon-si, Gyeonggi-do 16499, Republic of Korea

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ABSTRACT

Currently, as semiconductor packages are becoming increasing smaller with improved performances, many are being constructed using stacked structures. However, these types of packages are not easy to qualify owing to the potential swelling of the stacked layers. In this paper, we propose a new method for reliability testing that directly measures the adhesion strength using the swelling temperature to assess the reliability of the package. The swelling temperature is the temperature at which a peel-off occurs between the layers. The advantage of the proposed method in comparison with the traditional reliability testing methods is that the proposed method enables a quick assessment of the product reliability. Through testing and actual case studies, we found that the product reliability qualification can be determined solely by measuring the swelling temperature.

1. Introduction

Semiconductor technology continues to advance in order to support the ever-increasing demands for higher performances. Notable enhancements include increases in the memory capacity, data processing speed, and multi-functional products. These high-performance packages require ultra-fine form factor package and chip stacking methods; however, depending on the assembly methods, new failure modes such as swelling problems between the chips themselves, and/or between the chips and the printed circuit board (PCB) may occur.

This is because it is not always possible to completely eliminate interfacial voids from the attached surfaces; consequently, moisture can be drawn into the voids during repeated attachment and curing procedures, and a combination of this moisture and high temperature conditions causes the voids to swell. Therefore, as the packages become smaller and thinner, the total void area is controlled to occupy less than 5% of the chip area, although the void size control specification for manufacturing states that this figure should be 15% of the die area, as described in MIL-STD-883J Method No. 2030.

To address this package swelling problem, three types of screening tests are used. First, an ultrasonic inspection method may be applied to check whether voids exist on the adhesion layers; however, this method is not perfect because micro-voids are not always detectable. Next, the adhesion strength can be measured using a chip pull test; however, this method cannot be applied to stacked chip packages (SCPs) or package-on-package (POP) packages, if the chips or PCBs are very thin. Finally, if the 85/85% RH moisture sock and reflow tests are performed frequently for after-development monitoring, then it is possible to reduce the incidence of swelling. The challenge is that, although such tests are commonly used, their usefulness is limited because they are "go-no go" sampling tests that require several samples for reducing type I or type II errors [1,2]. As per the precondition testing method of the IPC/JEDEC J-STD-020E, the general test method for consumer products is for 168 h at an 85/60 RH with 3 reflows. These testing methods do not directly measure the package strength but instead use the stress applied before the failure as a proxy for the package strength. If the chance of failure in each lot in the high temperature and humidity qualification testing is 1/100 or 10/100 ea, the high temperature and humidity testing should be performed again in either case. Additionally, several experiments are required to determine the item that should be improved and the extent to which the temperature and humidity testing should be repeated. Even if a 0/100 ea occurs in this improvement test, a separate high temperature and humidity simulation should be performed to determine the degree of improvement. Accordingly, considerable time, several high temperature and humidity experiments, scanning acoustic microscopy (SAM), and adhesive interface analyses are required.

The objective of this study is to develop a novel method for package reliability qualification by directly measuring the temperature at which the swelling occurs, also known as the swelling temperature (Ts), between the layers because this temperature is representative of the strength of the package. This implies that Ts may be used as a package failure indicator to predict the package swelling quantitatively.

In Section 2, an explanation for the swelling is presented: its occurrence methodology and a method for determining Ts. We also provide the results of the Ts measurements for various packages to establish the measurement methods and moisture absorption standards. Finally,

* Corresponding author.
E-mail address: ghsong11@ajou.ac.kr (K.H. Song).

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the results of the Ts measurements based on the void size, a statistical analysis of the relationship between Ts and the reliability defects, and a prediction of the life expectancy are presented.

2. Package swelling

The package swelling phenomenon is shown in Fig. 1 (A). There are two types of swelling: The first type is caused by delamination under high temperature and high humidity conditions, when the adhesion strength is reduced because of contamination in the adhesion interface or problems in the adhesion structure and materials (see Fig. 1 (B)). The second type of swelling is caused by an increased vapor pressure in the voids, created when the epoxy molding compound (EMC) does not get completely filled under high temperature and high humidity conditions, as shown in Fig. 1 (C). Swelling occurs as follows: delamination occurs in the package at the photoimageable solder resist (PSR)/(EMC) interface, or at the PSR and die attach film (DAF) interface, or micro- or macro-voids remain in the adhesion interface.

The swelling temperature (Ts) was measured for the packages listed in Fig. 2 and the results showed that there were differences in the Ts measurements based on the package structures. In the case of the FBGA packages, Ts ranged from 275 to 297 °C. FBGAs A, B, and C have different numbers of chip stacks as per the function and they also differ slightly in terms of the thicknesses and x-y sizes. However, existing packages such as the small outline package (24SOP) and POP have very different structures from those of the FBGAs A, B, and C. The 24SOP contains one chip and its packaging is performed by EMC; the POP is a double stack package and therefore, is very thick.

The FBGA A package in Fig. 2 shows a Ts of 265–275 °C, lower than the Ts for the other packages. This is because the PCB Cu thickness in this package has a significant effect on the overall material properties for the PCB at high temperatures. The PSR and the core, having viscoelastic epoxy as their main ingredient, have an extremely low Young's modulus at less than 1 GPa; however, Cu maintains a high Young's modulus between 110 and 128 GPa, regardless of the temperature. When the Cu thickness is increased, the overall stiffness of the PCB also increases and this increases the likelihood of voids remaining in the DAF and PCB interfaces. A focused ion beam (FIB) analysis revealed the existence of a micro-void in the package, in the interface between the DAF and PCB layer, as shown in Fig. 3.

As shown in Fig. 4, for the EMC molded underfill (MUF) type, a flip chip BGA (FCBGA) package that has no voids at the interface, the adhesion strength can be weakened by thermal stress and vapor pressure, causing swelling. Additionally, there are defect modes that are attributed to slightly different forms that increase with the swelling. In the Fig. 2, Flip Chip BGA A Lots show wide range of temperature relatively, there were some instances wherein, the swelling occurred at lower temperature and others, where the swelling took time to develop.

As shown in Fig. 4, the defective lot samples had Ts values in the range, 260–267 °C, whereas, the normal lot samples had a range of 287–292 °C. These results show distinct differences in the temperatures at which the swelling occurred between the defective and normal lots. The temperatures at which the swelling occurred were marked as Ts.

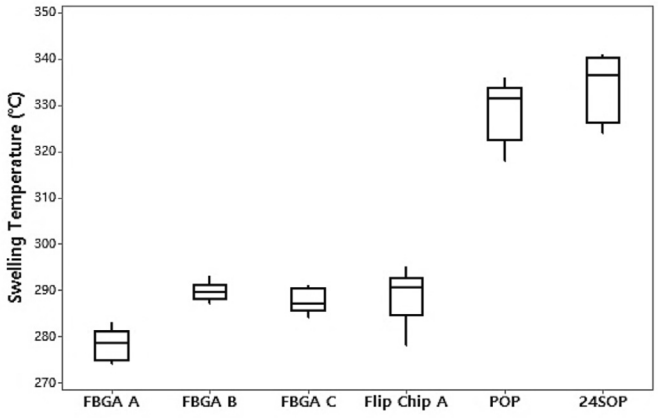

Fig. 2. Ts distribution for different package types.

Fig. 5 illustrates how a swelling occurs in an FCBGA package. Under high temperature and high pressure conditions, delamination first occurs at the EMC/PCB interface in the bump area. Then, as the delamination area increases, swelling occurs and cracks form in the chip or package in what is known as the "popcorn phenomenon" by increased thermal stress and vapor pressure [3–5].

Occurrence of EMC/PCB delamination in-between the bumps → increase in the delamination area → swelling occurrence → chip cracks by swelling.

An ultrasonic scan and microscopic interfacial analysis of the adhesion area were performed after an 85/85% RH reliability test. As shown in Fig. 6(A), a sample was selected from a lot in which delamination was detected. Then, a transmission electron microscope (TEM) was used to inspect the EMC/PSR interface in detail. Upon analysis, a micro boundary line was observed, 30–55 nm in width, exhibiting worm-type micro-voids. For comparison purposes, when a sample from a normal lot that did not exhibit swelling was analyzed, no such boundary line found between the layers, as shown in Fig. 6(B).

3. Swelling temperature (Ts)

It is essential to verify the presence of interface swelling as a result of thermal stress and vapor pressure between the layers of stacked packages. Consequently, reliability assessments of the possibility of a swelling occurring after long storage periods under high temperature and high humidity conditions are needed. The adhesion strength of a material with tiny voids in the interface was predicted to be relatively weak; however, it was difficult to measure the adhesion strength of stacked layers using a mechanical adhesion test because the layers were thin.

Our results show that the measured Ts were unique between 250 and 350 °C, according to the package structures or process conditions. To define the Ts values based on the package structure, material, and method, we reviewed the literature on the temperature characteristics of the materials that constituted the packages affected by swelling. To protect the integrated circuit (IC) chips in a package, an EMC with a

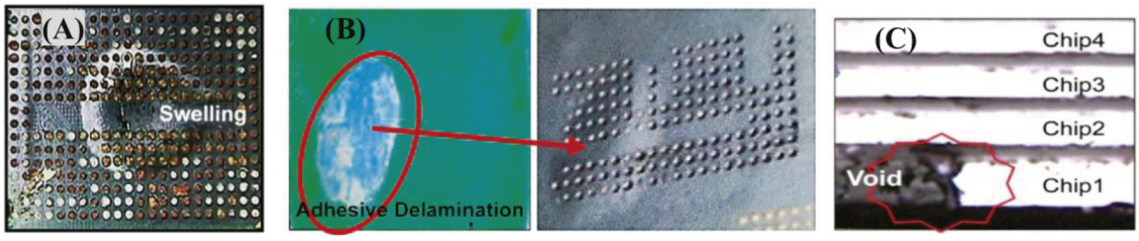

Fig. 1. (A) Package swelling, (B) die adhesive film delamination, (C) void in the EMC.

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