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# Characteristics of ESD protection devices operated under elevated temperatures



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#### ABSTRACT

In this paper, characteristics of electrostatic discharge (ESD) protection devices operating under ESD stress and various ambient temperatures are investigated. The devices considered are a P+/NW diode and several silicon controlled rectifiers (SCRs) including Lateral SCR (LSCR), Modified Lateral SCR (MLSCR), No Snapback SCR (NS-SCR), Low Voltage Triggering SCR (LVTSCR), and P-Substrate Triggered SCR (PSTSCR) fabricated in a 0.35 µm BCD (Bipolar-CMOS-DMOS) technology. Measurements are conducted using the Barth 4002 transmission line pulse (TLP) tester and the Signatone S1060 heating module, and the TLP I-V characteristics are analyzed in details. TCAD simulation is carried out and underlying physical mechanisms related to the effect of temperature on key ESD parameters are provided.

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### 1. Introduction

Electrostatic discharge (ESD) is a major reliability issue in the semiconductor industry, and ESD protection devices are frequently used to mitigate such concerns. As the technology advances, these devices become more susceptible to ESD-induced failures [1]. This is compounded by the fact that the assembly and/or operation of integrated circuits in some cases are taken place at elevated temperature, and the ESD protection designs become more complex due to the thermally-induced variations of ESD parameters [2]. Thus it is necessary to systematically and comprehensively analyze the characteristics of ESD protection devices to ensure they are suitable for operations under elevated temperatures.

Lin et al. [2,3] introduced the temperature-dependence steady-state and dynamic-state characteristics of some silicon-controlled rectifier (SCR)-based ESD protection circuits. They primarily focused on the triggering and holding behavior of such circuits. Meneghesso et al. [4] and Koo et al. [5,6] reported the holding voltages of new SCRs under high temperatures and explained the underlying physical mechanisms using TCAD simulation results. Other studies [7-18] looked into the ESD testing results under elevated temperatures to verify the temperature stability of the proposed devices. However, those papers only discussed the triggering and/or holding manners of their proposed SCRs under high temperatures and did not provide the underlying physical mechanisms and simulation results.

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In this paper, temperature-dependent characteristics of ESD protection devices including a diode and several SCRs will be analyzed. The transmission line pulsing (TLP) I-V curves will be measured, and key parameters such as the breakdown voltage V<sub>BD</sub>, trigger voltage/current V<sub>T</sub>/ It1, holding voltage/current  $V_H/I_H$ , failure current It2, on-resistance  $R_{ON}$ and DC leakage current will be studied and discussed. TCAD simulation were carried out to offer physical insights into the high temperature operations and key ESD parameters including the failure current, onresistance and DC leakage current, etc. under high temperatures are also very important and are characterized for the first time in our paper.

#### 2. Experimental result and discussion

The devices are fabricated in a 0.35 µm BCD technology. The measurements are targeted for the human body model (HBM) and are conducted using the Barth 4002 TLP tester with a pulse width of 100 ns and a rise time of 10 ns. The Signatone S1060 heating module is used to generate the different ambient temperatures of 300 K (25 °C), 400 K (125 °C) and 500 K (225 °C). The typical operating temperature requirement for electronics is up to 400 K (125 °C). However, the temperature requirements may vary for different applications. Our ESD devices were aimed for automotive applications which have a temperature requirement higher than 400 K. The temperature ranges of automotive electronics may extend up to 850 °C [19]. As such, the study of characteristics of ESD devices operating at temperatures higher than 400 K will be desired for such products. We will first characterize several SCRs that are targeted for different ESD metric, and followed by the study of a diode which is used widely for ESD applications as well.

2.4

2.3

2.2

21

500





Fig. 1. (a) Cross-section view of LSCR, (b) TLP I–V characteristics of LSCR, and (c)  $V_{BD}$ ,  $V_{T}$  and  $V_{H}$  versus temperature.

400

Temperature (K) C

2

20

19

18

300

Fig. 1(a) and (b) show the cross-section view and TLP I–V curves, respectively, of the lateral SCR (LSCR), a widely used and highly robust ESD protection device, under the three different temperatures. The variations of  $V_{BD}$ ,  $V_T$  and  $V_H$  with respect to temperature are shown in Fig. 1(c).

Fig. 2(a) and (b) show the simulated cross-section view of LSCR and simulated quasi-static I–V curves. The electric field at the NW/PW junction under various ambient temperatures is shown in Fig. 2(c).

The measurement results suggest that  $V_{BD}$  and  $V_T$  increase with increasing temperature which agrees well with the simulated I–V characteristics given in Fig. 2(b). This is because the triggering mechanism of LSCR is governed by the avalanche breakdown in the NW/PW junction and the thermal coefficient of the avalanche mechanism is positive vs. temperature. The electric field at NW/PW junction in Fig. 2(c) is captured at the same device voltage ( $V_{Device} = 20$  V) before the device

**Fig. 2.** (a) Simulated cross-section view of LSCR, (b) Simulated quasi-static I–V characteristics of LSCR with log scale y, (c) Captured electric field at NW/PW junction under various ambient temperatures.

С

triggering. We could learn from Fig. 2(c) that at the same device voltage before device triggering, the electric field at the breakdown junction decreases when temperature goes up, which suggests that the breakdown voltage, required to reach the critical electric field increases with elevated temperature. This mechanism applies to all the ESD protection devices whose device triggering are governed by the avalanche breakdown.

On the other hand,  $V_H$  decreases with increasing temperature which is also perfectly matched with the simulated I–V characteristics presented in Fig. 2(b). This is because increasing the temperature increases the intrinsic carrier concentration, which in turn decreases the barrier of PN junction in silicon [20]. Thus, the higher temperature results in a lower V<sub>H</sub>. This theory works with all the SCRs we discuss in this paper. However, the free-carrier mobility decreases, which results in an increased resistivity, when the temperature goes up. Thus, the turn-on resistance R<sub>ON</sub> increases with increasing temperature. Download English Version:

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