Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Thermo-mechanical simulation of PCB with embedded components

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ARTICLE INFO

Article history:
Received 3 June 2016
Received in revised form 21 July 2016
Accepted 22 August 2016
Available online xxxx

Keywords:
Finite elements simulation
Printed circuit board
Thermo-mechanical coupling
Embedded components

ABSTRACT

In recent years, in order to increase density and performance of electronic boards, components are embedded in internal layers of printed circuit boards (PCBs). The reliability of this new technology has to be investigated to ensure the working of the electronic boards submitted to harsh environment and long mission profiles. To study the thermo-mechanical behavior of these boards, finite element simulations have been performed. It is observed that embedded passive chips are subjected to complex loading during the lamination process, due mostly to shrinkage of the resin, differences in material properties and also because of temperature excursion. The effects of material parameters and of the geometrical configuration are investigated in details. It will be shown that the generated stresses are not critical for the passive chip size considered in the present work.

1. Introduction

The trend of miniaturization in electronics industries has led to a necessary increase of density of interconnections. Indeed the size of the boards has to be reduced or at least the number of Input/Output (I/O) has to be greater. The printed circuit board (PCB) is the carrier of surface-mount devices (SMD) for instance. Since the density of SMD is so high on current electronic devices, it becomes clear that new solutions to save some surface left have to be developed and validated via a large effort of research. An innovative solution proposes to incorporate passive and/or active components onto inner layers of PCBs and connect them through laser microvias [1–3]. This new technology has the advantage of increasing the connections, reducing the number of solder joints which are sources of failure [4,5] and improving the electrical performances as well. However, these assemblies are not immune to failure risks due to thermo-mechanical loading during manufacturing and operation. The right level of reliability with regards to mission profile has to be demonstrated before implementing this technology into a product.

Since the technology is developed by few actors, very recent studies have been carried out in this area. Atli-Veltin et al. [6] have studied the thermo-mechanical reliability of a resistor and a capacitor embedded in PCB during the manufacturing stage, by using a finite element analysis. The authors have simulated the temperature variation during the lamination steps and showed that the cooling step causes compressive stresses in the components. They concluded that the risk of cracks is low because of the great compression strength of the components. Pletz et al. [7] demonstrated by analytical method that taking into account the shrinkage of the resin induces compressive stresses in the component. J. Stahr et al. [8] have simulated the embedding process to identify the high stress areas and the strain fields within an embedded package. They confirmed the conclusions of [6]. Schwerz et al. [9–11] have investigated two embedding processes. The authors named them SMT & Cavity or Microvia & Cavity. The main difference originates from the design of the electrical connection of the component to the copper path (solder joint for SMT & Cavity versus microvia for Microvia & Cavity). Based on finite element calculations, the authors are able to detect critical areas in the solder joint and in the microvias. They perform also environmental tests (>4500 thermal cycles in the range −55 °C/+125 °C) and compare SMT & Cavity process to the classical SMT technology. The authors observed that for the SMT & Cavity technology, the integrity of the solder is ensured (when compared to the classical SMT technology) because of the resin which creates a protective layer for the component and the solder. Nevertheless, they found that cracks propagate in the resin material, from the upper surface of the component toward the top layer (fiber reinforced composite). In their approach, the shrinkage strain due to curing is not accounted for. We propose to provide a further and deeper understanding of the stress development in the PCB with embedded components by considering shrinkage of the resin and of the prepreg. In our approach, the component is glued by some polymeric paste, see Bodin et al. [12]. Recently, Macurova et al. [13] studied the embedding of silicon die into the board. They carried out axisymmetric finite element simulations, taking

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http://dx.doi.org/10.1016/j.microrel.2016.08.016
0026-2714/

into account the package manufacturing. The lamination theory of plain woven structures is adopted to determine the orthotropic properties of the prepreg materials (epoxy resin with E glass fibers). The role of the mismatch of coefficients of thermal expansion and of the shrinkage of polymeric materials is investigated carefully. After processing, the curvature of the board is measured by X-ray diffraction method. The consistency of the predictions of the model with the experimental results validates the proposed approach. Macurova et al. [14] have tested different sizes of silicon die, from 1 mm to 12 mm length. They observed that the measured deflection is large with larger die. Analytical approach based on the Classical Theory of Laminates (CTL) has also been proposed. They found that the curvature prediction based on CTL is consistent only with large die. They also found that the shearing stress at the interfaces are only significant near the edges of the component and vanishes in the central area. In our approach, we concentrate on components with 1 mm length. We conduct finite element calculations (3D for the reference configuration and additional 2D simulations for the parametric study) to investigate the stress state in the component and also in the resin of the cavity.

The goal of our paper is to investigate by numerical means, the embedding process to determine the stress-strain fields in the board and in the vicinity of the passive components. As mentioned in the literature review, embedding process induces compressive stress in the components. The paper is organized as follows. Section 2 presents the process for the embedding technology. The sequential steps will be used as guideline and reproduced in the numerical simulations. The numerical model is developed in Section 3. Shrinkage and measured temperature evolution during the lamination step are accounted for. The evolution of the compressive stress in the component with respect to process parameters (cavity size, volume of the resin …) will be presented in details in Section 4. The reference configuration adopted in this paper incorporates two components in the same cavity. As already mentioned, we concentrate only on small components (with a typical length of 1 mm only). Finally, we investigate numerically the possibility of placing two different components in the same cavity. We also perform (experimental and numerical) thermal cycling ($-55\ °C \leftrightarrow +125\ °C$) to illustrate possible evolution of the mechanical fields in the PCB during lifetime.

2. Context and manufacturing process

In standard electronic boards, components (mainly SMD) are assembled by reflow soldering on the outer layers (top and bottom) of the PCB, as shown in Fig. 1. In order to increase signal integrity and interconnection density, a possible solution is to embed passive components inside the core of the PCB. Fig. 1b presents an assembled board where passive components have been embedded in the PCB.

Fig. 1c shows a sketch of the central layer of the PCB of Fig. 1b showing embedded passive chips. Several chips are grouped in a single cavity. They are placed in the vicinity of SMD components assembled on top surface to achieve better signal integrity, see cross-section of the PCB

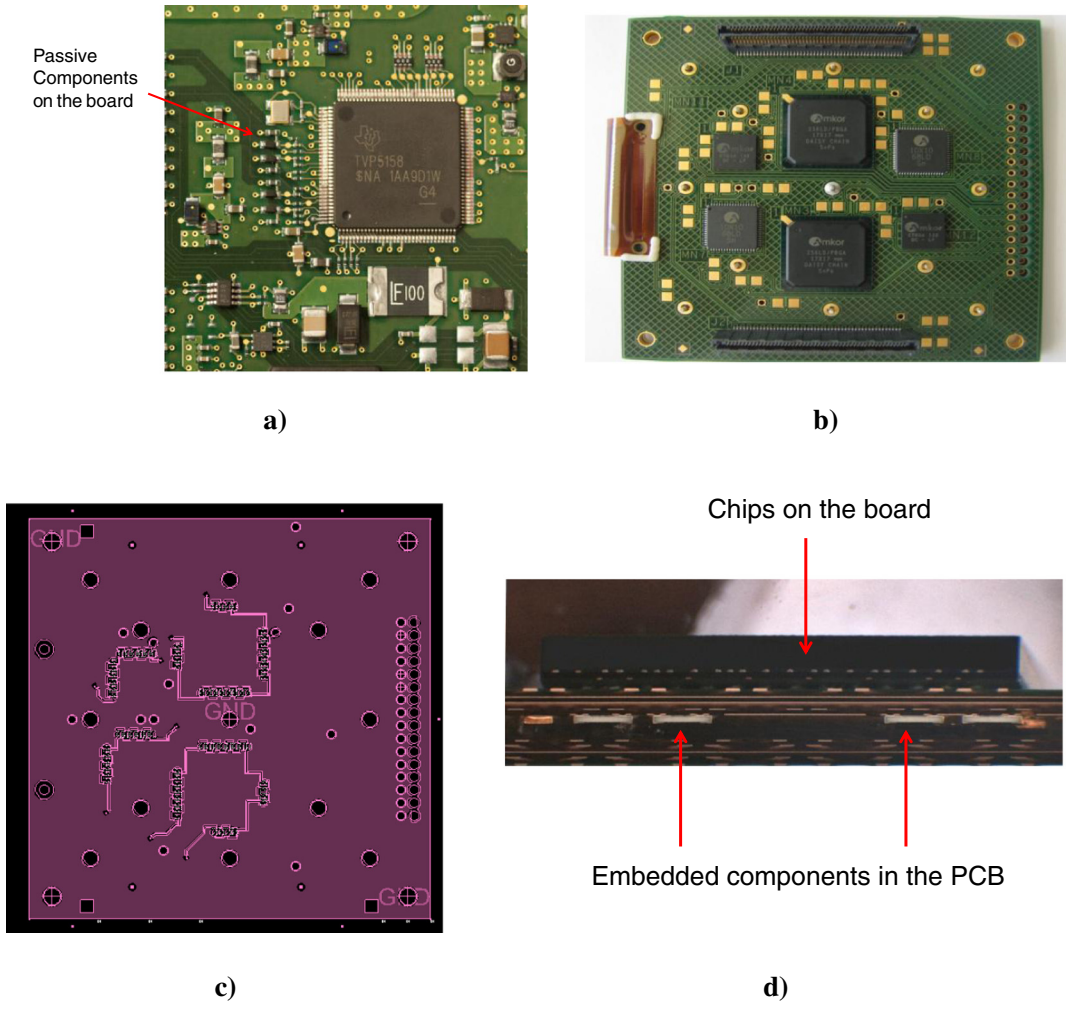

Fig. 1. a) Conventional board with passive components assembled on the top surface. b) Test vehicle with embedded passive components. c) Sketch of the central core of the PCB presented in b) where the passive components are embedded by group of several passives in a single cavity. d) Cross section of the PCB where the embedded passives are lying under the component assembled on the top surface.

Please cite this article as: W. Kpobie, et al., Thermo-mechanical simulation of PCB with embedded components, Microelectronics Reliability (2016), http://dx.doi.org/10.1016/j.microrel.2016.08.016