Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Lattice Boltzmann method study of effect three dimensional stacking-chip package layout on micro-void formation during encapsulation process

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ARTICLE INFO

Article history:
Received 19 February 2016
Received in revised form 22 June 2016
Accepted 4 July 2016
Available online xxxx

Keywords:
Lattice Boltzmann method
Topic:
Flip chip
Encapsulation
Micro-voids

ABSTRACT

The current study applied the lattice Boltzmann method to examine the effects of stacking chips layout to the micro-void formation in three-dimensional (3D) packaging. Three-dimensional 19-velocities commonly known as D3Q19 scheme is utilized in this study. Three different cases, which are different in layout design, are examined. For code verification purpose, an experimental work is also presented to compare the flow front results between numerical and experimental at different filling percentage. The numerical predictions compared well with the experimental results. Minor differences are observed in their flow front profile. The numerical findings identified the predicted locations of micro-void formation during the encapsulation process. The entrapment of micro-void was visualized clearly in the simulation because of the unbalanced molecular force at the interface during encapsulation. Knit lines were also identified at the interface between the flows that occurred in the encapsulation. Different layout of stacking flip-chips package have influence the micro-void in the package, which tended to form at the stacking chips region. The results show that the lattice Boltzmann method has a good performance in the IC encapsulation simulation.

1. Introduction

In the microelectronics industry, chip stacking technologies manipulate the Z height dimension to produce a high volumetric packaging solution for higher integration and performance. To enable package designers to accomplish their goals, 3D IC packaging [1] and three-dimensional (3D) integration [2] with through-silicon vias (TSVs) technologies were introduced. Reliable housings are require to maintain the device's reliability and protect thinned silicon chips and micro-size interconnection from the hazardous environment. Epoxy-moulding compound (EMC) was widely used in the encapsulation process for various IC packages such as thin quad flat packages (TQFPs) [3], thin profile small outline packages with wide side of lead on chip (TSOP II 54 L LOC) [4], stacking-chip scale packages [5], mould array packages [6] and moulded underfills [7]. During the encapsulation process, transfer moulding technology is used to feed the EMC into the cavity for covering the structures such as the wire bonding, silicon chips, paddles, solder bumps and passive components. However, the encapsulation process might cause the declining in IC package reliability and faulty such as interconnector fracture, warpage, deformation of chips and void formation. The epoxy is injected at the inlet gate, simultaneously covering and underfilling the chip. The gap between the chip silicon has to be completely filled with EMC in order to protect life of the chip assembly.

In the industry, package reliability has always been an interest among researchers and engineers. Ho et al. investigated the reliability issues of flip-chip packages through Moiré interferometry [8]. The evolution of area-array interconnects with high input/output (I/0) count and power dissipation made thermal deformation an important reliability concern for flip chip packages. Therefore, they proposed the Moiré interferometry to understand of this thermo-behaviour of flip-chip packages. They found that underfilling process reduce the shear strains of the solder balls but lead to delamination of the underfill interfaces. The study also shows that the die-fillet corner is a critical region with local stress concentration in the package. Zhong et al. examined the reliability of ball grid array (BGA) solder joints based on the effect of multiple reflow processes [9]. The study related to the mechanical behaviours and microstructures of BGA solder joints against organic solderability preservatives (OSP) coated copper pad on fiberglass (FR4) substrate after multiple reflow process. They reveal that SACI solder joints provide higher shearing strength compare to the SAC and SP joints during multiple reflow. However, the increase in number of reflow cycles does not significantly change the shearing force of these three types of solder joints.

Incomplete filling or air voids is one of concern during encapsulation process. Many aspects could have affected the severity of void formation such as chips layouts, thickness and the pressure. Publications regarding

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http://dx.doi.org/10.1016/j.microrel.2016.07.002
0026-2714/

factors contributing to void formations have been conducted using finite volume method (FVM) based software, ANSYS. Song et al. reported the prediction of air void during curing process for BCB bonding using experimental observations [10]. These voids if left unnoticed may reduce the bonding strength, decrease hermetic capability and could influence the yield and reliability of the package. Ong et al. studies the effect of microbump pitch on the formation of voids [11]. It was shown that air voids usually occur at the vicinity of microbump edge. Khor et al. conducted a numerical analysis on the effect of solder bump arrangement on capillary driven flip chip underfill process [12]. They found that middle empty layouts contributed to highest void formation due to deformation of the center region and packed solder bumps. Both studies are conducted on macro-scale level (finite volume method) without taking into account the effect of particle interaction forces on the micro-scale level. The air void formation requires deeper understanding of the strength attraction and repulsion at the particle level. Current study presents the application of lattice Boltzmann method (LBM) to the micro-scale flow simulation of stacking chip layout on micro-void formation during encapsulation process. To the best knowledge of the authors, study of effect three dimensional stacking-chip package layout on micro-void formation has never been reported. There are already few researches on fluid flow simulation through BGA in the past but they are mainly focused on finite volume method (FVM) and finite element method (FEM) [13].However, the FVM and FEM are limited to macro-scale level only.

The LBM uses a simplified kinetic equation for simulating fluid flow. The LBM is found to be more stable during the calculation and the results obtained are comparable with other finite volume based software such as FLUENT [14]. The LBM also has the capability to reduce time consuming derivations of the velocity data when simulating shear-dependent non-Newtonian flows, including fluids [15]. In the case of rising bubble flows, spurious currents and interface capturing, the LBM performs better than FLUENT [16]. The advantages and disadvantages of LBM are summarized in Table 1.

In recent years, LBM has been used in diverse applications including in electronics, structural and biomedical fields. The LBM method has been used to solve several of fluid transport phenomena [22]. This new computational tool was used in complex geometries [23], incompressible fluid flows [24,25] and two-phase flow [26]. Chemical reaction in micro and mesoscopic flow [27] was also shown to be applicable to simulate due to kinetic nature of the LBM method. In this paper, a stacked chip encapsulation simulation method is established based on three-dimensional LBM D3Q19 velocity set. The interaction between epoxy mould and stacked chip is modelled based on free surface flow model. The present study considers the 3D IC package with three different layout of stacking chips. The effects of the EMC flow behaviour in the stacking chips and the pressure and velocity on the stacking chips are also investigated.

Table 1
The advantages and disadvantages of LBM.

Advantages	Disadvantages
In general, the implementation of LBM is much easier compare with FVM/FEM [17]	LBM consumes more memory and performs more floating point operations per time step compare with FVM/FEM [18]
LBM have the capability on fast computational speed and high accuracy [19]	Combination of high and low resolution area, or application of curved grids is difficult due to limitation on regular square [20].
LBM offer flexible model accuracy and computational efficiency for design simulation tool to be able to simulate flows in the continuum and transition regimes [21]	Only a few commercial softwares have been developed such as powerFLOW and XFlow.

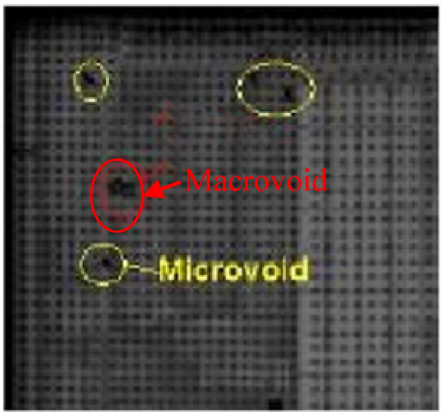

Fig. 1. Micro-void and macro-void trapped in the cured epoxy. The micro-void size is less than 100 μm and the macro-void size is larger than 100 μm [31].

2. Problem description

The main concerns during encapsulation process are the IC package failure due to cracks and fractures at the interconnector, the void formation and the critical displacement of the silicon chips. During the encapsulation process, reduced chip size with increased I/O counts could also cause serious wire sweep. The voids trapped reduce the overall package and board level reliability. There are two types of void sizes in the package which are micro-void and macro-void as shown in Fig. 1. Voids are usually described as the area they cover in the plane of the die. Macro-voids are the large sized voids commonly seen on X-ray during inspection. The size range for macro-voids typically from 100 to 300 μm in diameter while for micro-voids smaller than 100 μm in diameter [28]. During the quality control specification, macro-voids are not acceptable while micro-voids are passed the specification. However, micro-void may effected the overall package reliability for further thermal stresses. Fig. 2 illustrates the schematic diagram of encapsulation process for the flow. Commonly, the increase in the number of stacking chips and layout also increases the package volume. Hence, a longer filling time is needed to completely fill the mould and micro-void formation may occur in the package during the process, especially at the tight space between the stacking chips.

In the first part of the current study, the capability of the Palabos software in handling multiphase flow problems was validated with the previous experimental results [3]. Palabos is an open-source CFD

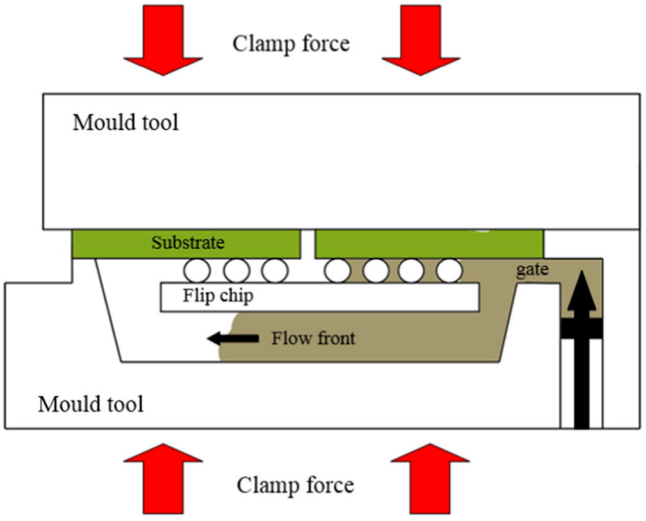

Fig. 2. Flip chip encapsulation process.

Please cite this article as: M.H.H. Ishak, et al., Lattice Boltzmann method study of effect three dimensional stacking-chip package layout on micro-void formation during encapsulati..., Microelectronics Reliability (2016), http://dx.doi.org/10.1016/j.microrel.2016.07.002