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Impact of thinning stacked dies on the thermal resistance of bump-bonded three-dimensional integrated circuits

Samson Melamed *, Naoya Watanabe, Shunsuke Nemoto, Haruo Shimamoto, Katsuya Kikuchi, Masahiro Aoyagi

National Institute of Advanced Industrial Science and Technology (AIST) Central 1, 1-1-1 Umezono, Tsukuba 305-8560, Japan

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ABSTRACT

In three-dimensional integrated circuits (3DICs) aggressive wafer-thinning can lead to large thermal gradients, including spikes in individual device temperatures. In a non-thinned circuit, the large bulk silicon wafer on which devices are built works as a very good thermal conductor, enabling heat to diffuse laterally. In this paper we experimentally examine the thermal resistance from an active on-chip heater to the heatsink in a two-tier bump-bonded 3D stacked system. A simplified structure is introduced to enable such measurements without the time and cost associated with the full fabrication of such a system. Die thinning is seen to have a pronounced effect on the thermal response, which can adversely affect system reliability. Thinning the top tier from 725 μm to 20 μm resulted in a nearly 4 times increase in the normalized temperature rise of the heater of our test chip.

1. Introduction

In three-dimensional integrated circuits (3DICs) aggressive wafer-thinning can lead to large thermal gradients [1], including spikes in individual device temperatures [2]. In a non-thinned circuit, the large bulk silicon wafer on which devices are built works as a very good thermal conductor, enabling heat to diffuse laterally. When the wafer is thinned, the heat generated by individual devices can no longer spread out as well, with the result being "hotspots" in the temperature profile. In [2] it was found that single clock buffers could create hotspots when they were located in the upper tiers of a fully-depleted silicon-on-insulator (FDSOI) 3DIC. Torregiani et al. have done a simulation-based study on the impact of various parameters on the size and temperature of dies as thin as 20 μm [3]. Santos et al. simulated the effects of substrate thickness and die bonding options on a memory-on-logic 3D circuit and found increased temperatures at decreased thicknesses [4]. Kato et al. investigated how thinning the die results in increased hotspot temperature [5]. The effects of high temperatures on semiconductor devices include reduced carrier mobility, increased subthreshold leakage [6], and decreased mean time to failure due to electromigration [7]. Increased temperatures not only directly affect system reliability, but also make it increasingly challenging to design working circuits: changes in device performance with temperature necessitates the consideration of on-chip temperature variations when attempting to obtain timing closure in digital circuits [8,9].

In a bump-bonded system, two or more wafers or dies are vertically stacked. Through silicon vias (TSVs) are placed into thinned upper tiers to allow for vertical electrical connections. Bump bonds are then used to connect between a lower tier's electrical wiring and an upper tier's TSV. The gap caused by these bump bonds must be filled with an underfill material, which typically has a poor thermal conductivity, around two orders of magnitude lower than that of silicon.

TSVs are typically limited to an aspect ratio (depth to diameter) of approximately 20 or less. For instance, at a wafer thickness of 20 μm, the TSVs will need to have a diameter of approximately 1 μm or more. This is significantly larger than a traditional back end of line (BEOL) via, meaning that routing vertically between tiers comes with a large overhead in area. There is, therefore, a significant interest in thinning the tiers that contain TSVs so that the TSVs can be sized more similarly to traditional vias. The downside to this, however, is that thinning the tiers increases the lateral thermal resistance of the individual tiers in the system by removing much of the bulk silicon.

It should also be noted that the handling of thinned wafers is significantly challenging. Die thinning can be accomplished on fully fabricated wafers by first mounting them on a support glass substrate. This allows for the sample to stay rigid during thinning, and allows for adding microbumps and dicing.

Oprins et al. have previously conducted measurements to investigate temperature changes in hotspots caused by varying densities of TSVs in a system with thinned wafers that were hybrid-bonded with Cu-Cu bonds and a thin dielectric layer [10]. In this paper we experimentally confirm the normalized temperature increase (temperature increase divided by power) for a heater in a simplified stackup designed to replicate the thermal environment of a bump-bonded system. We

* Corresponding author.
E-mail address: samson.melamed@aist.go.jp (S. Melamed).

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have chosen not to include individual TSVs and bumps, as their location will be design-dependent. By not including these layout-dependent objects we have formulated a general worst-case scenario as a first step. We have measured the normalized temperature increase for the heater for upper die thicknesses from 725 μm (unthinned) to 20 μm.

The remainder of this paper is organized as follows. In Section 2 we discuss bump-bonded systems and our simplified structure for recreating their thermal environment. In Section 3 we describe the heater chip we have designed. In Section 4 we give the measurement results.

2. Background

A sample bump-bonded stack is shown in Fig. 1(a), with a heater embedded into the top silicon chip. The system is composed of two tiers. The top tier will need to be thinned in order to insert through silicon vias (TSVs) to provide for electrical connections between the top and bottom tiers. When the top silicon chip is thick, heat from the heater can easily spread out laterally, and then pass through the underfill/bump joint layer in order to reach the heatsink. The underfill/bump joint layer typically has a thermal conductivity approximately two orders of magnitude less than that of silicon. When the heat can spread out laterally first, the heat can then pass through the underfill/bump region in parallel over a wide area, which presents a relatively low thermal resistance. When the upper silicon wafer is thinned, however, there is no longer a low resistivity path for the heat to initially spread laterally: the thinned wafer has a much higher lateral resistance than that of the unthinned wafer. This is most easily understood by looking at the equation for the thermal resistance of a simple block of material:

$$R_\theta = \frac{l}{A \times k} \tag{1}$$

where l is the length of the block on the path parallel to the heat flow (m), A is the cross-sectional area of the block perpendicular to the path of the heat flow (m^2) and k is the thermal conductivity of the block (W/m·K). For a thin slice of the system of Fig. 1(a) we find that as the upper die is thinned the cross-sectional area from heater laterally along the upper Si chip decreases, indicating an increased resistance to lateral spreading. Should the underfill/bump joint layer have a similar thermal conductivity to silicon, this would not be an issue, as the heat could immediately move through the underfill/bump joint layer and continue spreading in the bottom chip. Since the underfill/bump joint layer has a high resistance, we expect to see that thinning the top tier will significantly increase the thermal resistance from the heater to the heatsink.

3. Methodology

In this section we first describe a simplified stackup that can be used to replicate the thermal environment of the system in Fig. 1(a) without fabricating TSVs and bump joints. We then describe the test chip that we have fabricated to experimentally determine the thermal resistance from the top heater to the heatsink for various thicknesses of the upper Si chip.

3.1. Simplified model

We will begin by describing the fabrication challenges to building the bump-bonded system shown in Fig. 1(a) and then explain our approach to create a simplified model of this system.

In general, the upper limit for the aspect ratio of TSVs that can currently be fabricated is approximately 20:1. This means that for the non-thinned case where the Si substrate is 725 μm, we would need to use TSVs with a diameter larger than 35 μm. While such a system could be fabricated and then thinned to various thicknesses to allow for a direct comparison, it would not reflect how a thinned system would actually be built to take advantage of the smaller TSVs possible due to the thinned die. That is, at a Si substrate thickness of 20 μm it is expected that TSVs of approximately 1 μm in diameter could be fabricated, which is significantly closer to the size of traditional vias. Therefore, for each thickness that we need to investigate, we would theoretically need to first thin the upper tier, and then insert appropriately sized TSVs. These chips would include layout-dependent effects based on the exact location of the TSVs and bumps. As a first step, we have chosen to remove the TSVs and bumps to create a worst-case thermal environment to aid in an investigation of the effects of thinning, while still staying true to the thermal properties of the non-simplified system.

For an actual system that does include TSVs, the impact of TSVs on the thermal conductivity of the substrate is expected to be low in a system where a bulk silicon process is used, as the thermal conductivity of Si (approximately 155 W/m·K at room temperature) is generally only around a factor of two from that of higher conductivity metals used to fill TSVs (approx. 200 W/m·K to 400 W/m·K). A real circuit would not have a TSV fill of 100%, meaning that the actual effect on the thermal conductivity by adding TSVs to the substrate would be by less than a factor of two. A fill rate of 25% is on the very high end of what is feasible, due to concerns over stress in neighboring circuits as well as the need to ensure that space exists for the circuits themselves in addition to the TSVs. We will use a 25% fill for the purposes of establishing a reasonable upper limit on the substrate thermal conductivity with TSVs. The parallel equivalent model (i.e. weighted averages) will yield the upper limit on the thermal conductivity:

$$k_{eq} = A_{TSV}k_{TSV} + (1-A_{TSV})k_{Si} \tag{2}$$

where A_{TSV} is the fractional portion of area of the TSVs (between zero and one) and k_{TSV} and k_{Si} are the thermal conductivities (W/m·K) of the TSVs and Si, respectively. We will assume that TSVs are filled with copper of thermal conductivity $k = 401$ W/m·K and the remainder of the substrate is silicon with thermal conductivity $k = 155$ W/m·K. Using Eq. (2) a TSV fill of 25% yields an equivalent thermal conductivity of 216.5 W/m·K, which is only around 40% higher than the thermal conductivity of Si. A 4% TSV fill, which has been proposed as a realistic value for TSVs in [11], would yield an equivalent thermal conductivity of 164.8 W/m·K, which is only 6% higher than the thermal conductivity over silicon. The TSV liner is generally made from a low conductivity material, which means that the actual equivalent thermal conductivity will likely be even closer to that of silicon. We therefore find that simplifying the model by removing TSVs in a bulk Si bump-bonded system

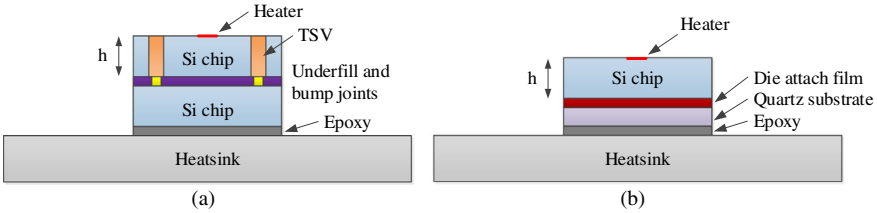

Fig. 1. (a) Two-tier stacked system with underfill and bump joints. (b) Simplified structure for thermal measurements including a layer with poor thermal conductivity (die attach film) under the top chip to mimic the thermal properties of underfill and bump joints as well as a quartz substrate to increase temperatures to a range that is more easily measurable.

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