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# Enhanced thermal characterization method of microscale heatsink structures

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ABSTRACT

In the frame of thermal management of electronic devices, finding efficient cooling solutions for next generation equipment is an emerging topic. If a new or improved solution is presented it always requires efficient characterization methods to prove the benefits compared to its predecessor. In case of microscale heatsink structures which are integral parts of modern chip or package level cooling concepts, an efficient measurement method is needed to analyse the performance of structures with different layouts and/or manufacturing technologies. This paper presents an enhanced thermal characterization method of microchannel based cooling structures, determining relevant partial thermal resistances from structure functions obtained by thermal transient testing. Our prior microscale heatsink characterization method was recently improved, accounting e.g. for possible non-idealities of the heat transfer processes. This paper presents how we have improved our measurements setup in detail to deal with these phenomena compared to the previous setup.



## 1. Introduction

Due to the increasing integration of components per unit area and the 3D packaging technologies the elevated dissipation of integrated circuits induce elevated die(s) temperature [1,2,3]. In order to keep the rising temperatures within safe limits several cooling solutions evolved together with the scaling. Today the conventional air-cooling techniques are reaching their limits, thus new designs are investigated in order to be able to cope with the increased heat flux and to keep die temperatures in an acceptable range. One proposed solution is the application of special cooling structures where fluid flows through microscale channels formed in the substrate by either wet- or physical-etching (e.g.: reactive-ion etching) directly. The main benefit of the integration of these cooling structures is the lower thermal resistance between the dissipation area (junction) in the substrate and the ambient.

The thermal resistance of the integrated microscale cooling structures depends on several properties of fluid dynamics – e.g.: the flow rate and the exact geometry of the channel structures (dimensions, 3D layout etc.). The precise determination of the thermal resistance at different fluid flow-rates is mandatory in order to validate the simulation and/or analytical calculation results and prove the applicability of the cooling structure.

In the first approach these structures were used only for cooling purposes, but in several cases they could be applied also in thermal management solutions (e.g.: homogenization of the temperature distribution along the die surface or among dies in a stacked die structures). This kind of management is essential in some cases, because the main source of functional errors in digital integrated circuits is the temperature inhomogeneity, whereas the delay of standard digital cells is varied by the temperature change [4,5,6]. In case of clock distribution networks (CDN) of modern processors [7,8] the dynamic clock skew minimization demands temperature changes within the smallest possible range. In case of 3D packaging (e.g.: stacked dies) this problem is more serious.

In this paper an enhanced thermal characterization method is presented in detail which is aimed at the identification of the partial thermal resistances of different microscale heatsink structures. Several previous papers [9,10] presented the basic idea which could be successfully applied to determine the flow-dependent thermal properties of the microscale cooler structures, but the validity and repeatability of these methods were problematic. For example, in [10] the authors mentioned that it was not possible to determine the contribution from the individual components of the total unit thermal resistance. Several sources of inaccuracy were neglected and as a consequence the measurement results differed from the results of the CFD simulation and analytical calculation. In this article these sources of inaccuracy are identified and the difference between the results obtained by the new, enhanced thermal characterization method and the results of the former measurements is discussed. The results are also compared to the CFD simulation results for cross-verification purpose.

### 1.1. Realized microscale cooling device

The experimental samples were formed in a single side polished wafer, sliced with lateral dimensions of 15 × 15 mm. The channels were etched on the polished surface in radial directions as shown in Fig. 1 [12,13]. At the intersection – in the middle of the chip – a cavity

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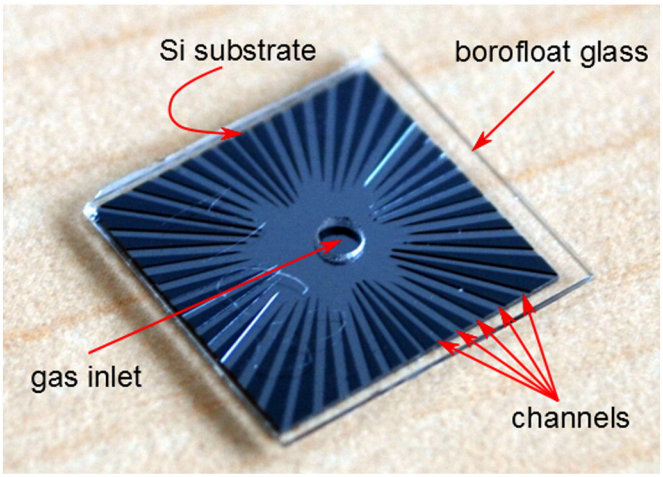


**Fig. 1.** Microscale heat exchanger device.

with a diameter of 4 mm was formed for the gas inlet. The channels on the polished side of the wafer were closed by borofloat 33 glass attached by anodic wafer bonding. For the gas inlet a hole with the diameter of 1 mm was cut into the closing glass substrate by laser ablation.

## 2. Methodology

Our characterization method is based on thermal transient testing [14] which also forms the basis of several JEDEC (Joint Electron Device Engineering Council) standard test methods [15]. The advantage of thermal transient testing followed by structure function analysis [14] is the capability to define not only the whole junction to ambient or junction to case thermal resistance, but also the identification of the partial thermal impedance of every single element in the main heat path [16,17]. Thermal transient testing has already been successfully applied to the characterization of non-integrated microchannel heat sinks, and proved to be a powerful and reliable tool for their thermal characterization [18,19,20] assuming certain conditions. In these setups, a dissipative element was mounted over a heat spreader on top of the cooler device, while the bottom side of the cooler is interfaced to a cold plate. This way the one dimensional heat flow path can be measured by thermal transient testing and the thermal parameters of each layer can be determined.

In the case of microscale channel cooling structures former papers dealt with the question of parallel heat flow paths which could be determined and eliminated, but the dependence on the fluid flow properties of such a shunting resistance was neglected [21]. As it can be seen in section 4 of this paper, our investigations proved that the parallel heat flow path represents a flow-rate induced heat path which adds a systematic error to the measurements results, totalling in more than 50% difference between measured and simulated data. The aim of our work is to eliminate these side effects and reduce the error of the measurement into an acceptable level and create a valid and reproducible method.

The scheme of the former measurement setup with the mounted dissipator, the cooler device, the heat spreader, the air supply, etc. (Fig. 2) was published in [21]. However, in order to carry out the measurements accurately the following considerations have to be made.

First of all, the overall thermal resistance of the whole measurement structure can be easily identified by measuring the temperature change response for a power step. In this case, the microscale cooling structures has to be attached to an active device for example to a conventional power transistor. After powering up the transistor its temperature change has to be measured and knowing the applied power step and the temperature rise of the junction, the $R_{thja}$ junction-to-ambient thermal resistance can be calculated as:

$$R_{thJA} = \frac{\Delta T_j}{\Delta P} \tag{1}$$

After obtaining the overall thermal resistance for the whole structure at zero flow-rate, the measurements have to be repeated at different (volumetric or mass) flow-rates of the coolant gas, which will result in the thermal resistance (or thermal conductance) vs. flow-rate characteristic(s). However, one must be aware of the temperature dependence of the forward voltage of the emitter-base junction temperature dependence is a non-linear sensitive parameter (TSP). Its sensitivity (or the K-factor) has to be identified in a separate calibration process.

The problem with this simple and straightforward method is that the thermal resistance identified this way includes all thermal resistances of the heat flow path (in our case the thermal resistance of the transistor, the thermal resistance of the copper heat-spreader, the thermal resistance of other supporting structures, etc.). To overcome this problem thermal transient testing has to be performed, which enables the separation of each structural layer in the heat flow path by deriving the structure function from the transient results (Fig. 3).

Since the recorded thermal transient curve contains all available information about the junction-to-ambient heat-conduction path the one-dimensional heat flow must be ensured. It means that the majority

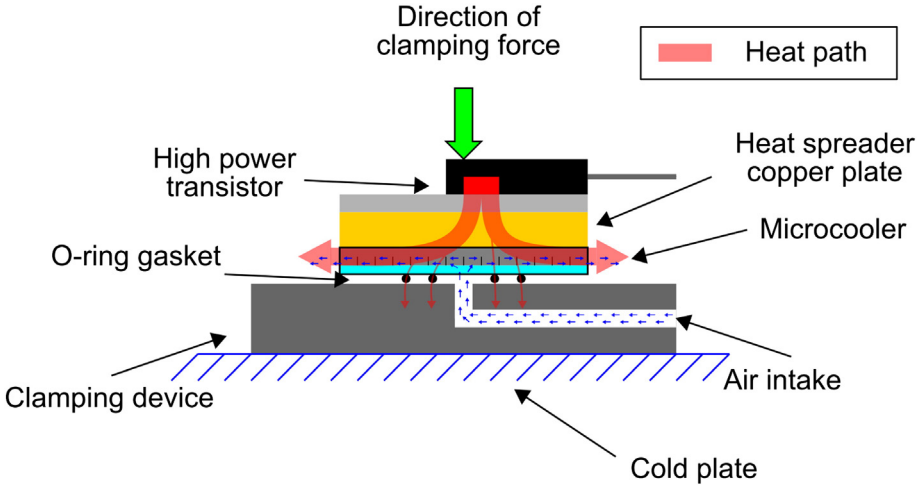


**Fig. 2.** Core of the former measurement setup [21].

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