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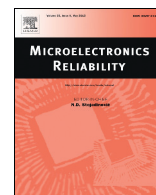

Multilevel logic and thermal co-simulation

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A R T I C L E I N F O

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A B S T R A C T

While the semiconductor industry makes progress in every year integrating more components on a single die and stacking them, manufacturers face great challenge as the dissipated power densities reach the limits of current cooling solutions. Since peak temperature and temperature gradients influence the functional behavior of the ICs, co-simulation of the logic function and thermal behavior can help to assess the overall performance of the system at various stages of the design flow better. Logi-thermal simulators (extending the concept of the transistor level electro-thermal simulation of integrated circuits to higher abstraction levels) can predict the dissipated power based on the switching activities of the system, consider the local temperature dependence of certain circuit properties and calculate the temperature distribution across the chip consistently.
This paper presents a logi-thermal simulation framework that allows to couple logic simulators and thermal solver engines to facilitate the co-simulation of high level functional and thermal behavior of digital circuits, both on gate level and register-transfer level. We show examples by integrating SystemC with the thermal simulator SUNRED, and comparing the results of a gate level logi-thermal simulation and logi-thermal simulation obtained with the register-transfer level description of the same system.
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1. Introduction

With the continuous evolution of the semiconductor industry, more and more complex integrated circuits can be manufactured, which has been predicted by Moore's law [1] and Dennard scaling [2]. With the shrinking minimal feature size, increasing parasitic effects lead to various design bottlenecks.

Today, thermal issues represent one of the biggest performance barriers for high-end chips. Cooling vertically stacked ICs became difficult due to the high heat flux density and increased thermal resistance caused by the low thermal conductivity die attach/interposer layers and the related thermal interfaces among the stacked dice. In such 3D integrated solutions micro-fluidic cooling offers a workaround to the heat-removal problem [3]. During the design process, several power, timing, and temperature estimations have to be made to explore the design space and find the optimal design points. Electro-thermal simulation uses transistor-level circuit models, thus it is not viable for design space exploration for large digital ICs, therefore coupling the simulation of the functional behavior with the simulation of the thermal performance needs to be raised to higher levels of abstraction, e.g. to gate level or above. Design costs and the design cycle can be reduced by enabling thermal and power aware simulations earlier in the design process.

Logi-thermal simulation paradigm is based on the idea that the dissipation of a digital circuit is determined by its switching activities and certain parameters of the circuit operation depend on the temperature. In the first implementations of the *logi-thermal simulation paradigm* the abstraction level of the electrical operation's description was raised from the transistor level to logic gate level [4,5]. In traditional electro-thermal simulation performed by the so called *direct method* the physical environment of the electrical circuit is mapped to a thermal network model, thus both the electrical network and the thermal environment are treated on the same abstraction level. In logi-thermal simulation the homogeneous representation of the digital circuit and its thermal environment is not possible, therefore a method known in traditional electro-thermal simulation as *simulator coupling* is used: a logic simulation engine and a thermal simulation engine are connected in a loop.

Assuming a gate level description of the logic circuit, results of the logic simulation engine combined with the layout of the circuit provides the *event density*, which, in conjunction with an appropriate *energy model* of the switching events, can be converted into a *dissipation map*. This serves as an input for the thermal simulator which in turn provides the corresponding *temperature map*. Using local temperatures of the logic gate instances, the temperature dependent parameters of their corresponding logic models are updated. After this update, the logic simulation in subsequent time window can be started and the iteration between the two simulation engines can be continued. Following the principles of logi-thermal simulation presented in [4], Timár et al. recently have implemented a logi-thermal simulation system in an industry standard IC design environment with the above described back-

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annotation of gate instances [5], and temperature dependent timing parameters [6,7]. With this simulation framework, it becomes possible to identify timing violations caused by the self-heating of the chip.

One major challenge in logi-thermal simulation is to bridge the gap between the time-scales of gate level logic operation (ns scale) and the thermal time-constants of packaged IC chips (from µs scale up to seconds). The other challenge is to bridge the gap between the levels of abstraction needed to describe the logic behavior (gate level, register-transfer level - RTL, system level) and the thermal operation (a model representing the 3D physical structure of the IC). A couple of years ago G. Nagy et al. started working towards a logi-thermal simulation system which was aimed at circuit descriptions with multiple abstraction levels using a unique, in-house logic simulation engine combined with a fast thermal simulator [8,9].

High abstraction level circuit description can reduce the simulation time, but it hides the details of the circuit behavior. While temperature dependent (gate) delay cannot be modeled on RTL, temperature distribution caused by the elements' power dissipation can still be analyzed and hotspots can be detected.

In this work (inspired by the ideas introduced in [7,8,10]) we describe how our initial results [11] were further developed.

- A new logi-thermal simulation framework has been introduced with generic interfaces to couple arbitrary logic and thermal simulator engines. In the present paper, we used SystemC as logic simulator engine and hardware description language, and SUNRED, an in-house thermal simulator engine [12].
- An improved RTL power estimation method, based on [30], has been fitted into the framework to predict the dissipation of RTL models.
- In a case study, we have compared the accuracy of the temperature maps obtained by the logi-thermal simulations of the gate level and RTL implementations of the same processor and also show the speed up of the co-simulation, which was possible by modeling the circuit on RTL.

Our paper is structured as follows: Section 2 discusses related work. Section 3 introduces the structure of our new framework and the interfaces to the logic and thermal engines. Sections 4 and 5 describe the RTL power estimation approach used in the framework and present a case study with the comparison of speed and accuracy of gate level and RTL logi-thermal simulations.

2. Related work

2.1. Thermal simulation of integrated circuits

Numerous researchers introduced modeling methods to calculate temperature and power related phenomena. Heat transfer equations have to be solved in order to determine the temperature distribution across the surface of the chip.

A popular approach is thermal network modeling which utilizes the duality between conductive heat transfer and electricity. The idea is to reduce the 3D physical structure to a network model of thermal resistances and capacitances. “Current” in such a model represents heat-flow and the “voltage” of each node in the resulting RC network represents a temperature value. A simple way of creating a thermal RC network representation of the 3D physical structure is to apply a spatial discretization scheme corresponding e.g. to the method of finite differences (used in the numerical solution of partial differential equations of the 3D physical heat-transfer problem). The resulting thermal RC network can be large (with a huge number of nodes), therefore either efficient solution methods are needed to threat such a network in an efficient way or techniques known as compact thermal modeling have to be used (see e.g. [13,14]) when a thermal RC network model of the physical structure is generated. In our work we use thermal RC network models obtained directly from the discretized physical structure, thus the spatial granularity of our approach is limited by the resolution of the physical structure's spatial discretization, and its thermal environment.

Thermal network modeling was used in HotSpot [15], SUNRED (successive network reduction algorithm) [12,16,17], and 3D-ICE [18,19,20]. The latter thermal engine can be used to simulate microfluidic cooling solutions as it is capable of modeling not only conductive but convective heat transfer as well. (Inclusion of modeling the cooling effect of convection in microchannels within a conduction mode thermal solver requires appropriate compact model of convective heat transfer. We treat this problem in a recent conference paper [21]).

These thermal simulators calculate the temperature distribution of the IC(s) based on the input information (dissipated power and area of the logic modules constituting the circuit). In our new logi-thermal simulation framework we have defined a standard interface allowing the application of any thermal simulator. Currently our in-house tool SUNRED is used as thermal solver and we also interfaced 3D-ICE to our framework called *LogiTherm*.

2.2. Co-simulation of logic and thermal behavior

Thermal related issues and the temperature of the die have become more significant as the dissipation density increased during the past years, therefore on-chip dynamic thermal management control solutions became common: modern microprocessors change the core clock frequencies based on the core temperature and the utilization of other components.

As this dynamic behavior is a function of temperature, it is no longer suitable to perform only static thermal analysis, but transient analysis based on the co-simulation of logic functionality and thermal behavior is needed.

As mentioned in Section 1, previous implementation of the logic and thermal co-simulation method by our team used standard cell libraries in conjunction with EDA tools to calculate the dissipated power, signal delay and temperature distribution. This logi-thermal simulator (called *CellTherm*) works at gate-level (see paper [5,6,7]), thus the resulted temperature map is detailed down to the level of standard cells; the calculated dissipations and delays are accurate. (The downside of this method lies with its advantage as the logi-thermal simulation of large systems can be slow due to the computational requirements.) The accuracy of this gate level approach was verified by transistor level Spice simulations [7], therefore in this paper gate level logi-thermal simulation is considered as a base line solution when speed and accuracy of an RT level logi-thermal approach is investigated.

A relatively recent experimental implementation of the logi-thermal simulation couples an in-house logic simulator engine with a thermal engine [8,10] with a solution aimed at resolving the conflict between the time scales of the logic operation and the characteristic of thermal time-constants. With this the co-simulation of the logic and thermal behavior of large systems can be performed quickly, as the logic engine supports multi-level abstraction, however, as the logic engine does not support a standard hardware description language, this solution cannot fit into any design flow in industrial engineering practice.

A different approach for co-simulating logic function and power/thermal behavior has been published in [22,23]. The introduced method uses highly abstracted functional models implemented in SystemC TLM, thus the dissipated power and the temperature can be evaluated together with the software executed by the functional model. High abstraction level is necessary to simulate how embedded software affects the thermal behavior of the system. The accuracy of the simulation is limited by the power and area estimation methods applied. A similar, high abstraction level co-simulation approach has been proposed by Kumar et.al [24]. These solutions are different from our method as they offer high level logic and thermal co-simulation (above RTL),

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