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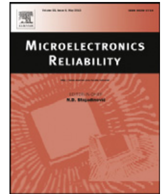

Analysis of aging effects - From transistor to system level

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ABSTRACT

Due to shrinking feature sizes in integrated circuits, additional reliability effects have to be considered which influence the functionality of the system. These effects can either result from the manufacturing process or external influences during the lifetime such as radiation and temperature. Additionally, modern technology nodes are affected by time-dependent degradation i.e. aging.

Due to the age-dependent degradation of a circuit, processes on the atomic scale of the semiconductor material lead to charges in the oxide silicon interface of CMOS devices, altering the performance parameters of the device and subsequently the behavior of the circuit. With the continuous downscaling of modern semiconductor technologies, the impact of these atomic scale processes affecting the overall system characteristics becomes more and more critical. Therefore, aging effects need to be assessed during the design phase and actions have to be taken guaranteeing the correct system functionality throughout a system's lifetime.

This work presents methods to investigate the influence of age-dependent degradation as well as process-variability on different levels. An operating-point dependent sizing methodology based on the g_m/I_D-method extended to incorporate aging, which aims at developing aging-resistent circuits is presented. Additionally, the sensitivity of circuit performances in regard to aging can be determined. In order to investigate the reliability of a complex system on behavioral level, a modeling method to represent the performance of system components in dependence of aging and process variability is introduced.

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1. Introduction

In many fields of application such as avionic, automotive and medical, a high operational lifetime and guaranteed functionality according to specifications is required. In order to meet the request for innovation in critical applications with high security requirements and the trend towards smaller feature sizes, reliability issues have to be addressed during the design process.

Apart from the variability of the manufacturing process, which results in e.g. mismatch and differing doping concentrations, the influence of age-dependent degradation mechanisms has to be considered. Aging effects can either occur as sudden events like time-dependent dielectric breakdown (TDDB) and electromigration (EM) or change the behavior of the device over time such as bias temperature instability (BTI) and hot carrier degradation (HCD) [1]. The shift of transistor parameters due to age-dependent degradation can result in a change of the systems performance. In decreasing CMOS technology nodes BTI and HCD seem to emerge as the most dominant reliability issues [2]. In contrast to EM or TDDB, the influence of BTI and HCD is more gradual and usually does not result in a sudden permanent damage.

Both HCD and BTI are caused by the accumulation of charges, so-called interface traps, in or near the gate-oxide resulting in a shift of transistor parameters such as the threshold voltage [1]. In the case of HCD, accelerated charges are injected into the gate-oxide and cause interface traps. Usually HCD is empirically modeled using a power law model presented in e.g. [1,3]. In contrast to this, two widely used modeling approaches are currently known for the BTI mechanism. One approach is based on the reaction-diffusion (RD) model, which was introduced in the 1970s [4] and has been accepted and extended in various publications [5,6]. An advanced BTI model uses capture and emission time maps for modeling the more recently discovered relaxation effect in BTI degradation. It was introduced by Huard and Denais [7] and is described in more detail in [8,9]. BTI is believed to be caused by the destruction of hydrogen-silicon bonds by charge carriers as well as highly energized charges being trapped in the oxide [1]. Experimental verifications and descriptions of all of these models are usually provided by the foundries.

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The prediction of impact on transistors and circuits caused by aging effects can be computed using commercial reliability simulation tools such as RelXpert [10], Eldo or Mosra [1]. Analyzing the influence of aging on a system requires the evaluation of every single transistor in the circuit, which is time consuming since the aging analysis is based on transient simulations to evaluate the stress conditions for each component. Furthermore, the interdependency of degradation effects with process variability has to be taken into account once realistic predictions of a system's reliability over lifetime shall be made. Simulation methods addressing process variability, as e.g. Monte Carlo approaches, already exist. However, commercial EDA-Tools do not cover these in combination with degradation effects so far [11]. This work mainly focuses on RelXpert as aging simulator, enabling simulation of degradation influence on CMOS transistors due to BTI and HCD. However, the proposed methods are independent of the degradation simulator, as long as the simulation results can be converted into a SPICE netlist including degraded CMOS devices.

A couple of reliability driven design schemes are described in literature for optimizing lifetime and degradation behavior [12–14]. Different methods exist, which exploit the available design space in order to yield a degradation-aware circuit sizing. In [12] the worst case distance (WCD) of a given performance characteristic is computed to be used as an input for an objective function, which also considers degradation and process variability. The optimization is done by maximizing the objective function (and WCD) for an arbitrary operating time and then modifying the fresh netlist until the desired specification is fulfilled [13]. The inability to retrace the decisions on why the dimensions of a transistor are altered is a major drawback of this method. A combination of transistor-level degradation simulation and reliability analysis on block and system-level is proposed in [15,16]. A deterministic reliability simulation flow is introduced, which uses a special simulation setup that is not available within commercial counterparts. Reliability aspects are ported from transistor up to system-level using behavioral modeling approaches, without focusing on a dedicated description language.

To ensure a reliable system operation, both, degradation and process variability, need to be considered at system-level, ideally without the cost of complex and long simulation runs. System level verification of complex analog and mixed-signal integrated systems is often performed using behavioral models instead of SPICE-level netlists. With a methodology at hand that allows the system designers to integrate degradation and process variability information into these behavioral models, a significant reduction of the simulation effort can be achieved, while the quality of the whole design flow is improved. In order to compute accurate results at system-level regarding degradation and its influence on system performance characteristics, it is important to transfer results from transistor level up to the system-level without loss of information. This abstraction of information can only be achieved by considering degradation mechanisms and process variability from transistor-level on and carefully porting this information across all design levels. This includes sizing of transistors [17], creating variability- and degradation-aware netlists [11] and finally generating behavioral models [18].

In this work, reliability is investigated on different design levels and methods enabling designers to take actions against aging effects are introduced. By utilizing the well known g_m/I_D sizing method in combination with the derivation of an operating point-dependent degradation, an aging-aware sensitivity-map (AAS-Map) revealing circuit's sensitivity to aging is developed. The proposed method is suitable for determining appropriate transistor sizing of analog circuits. The principle advantage of the proposed methodology is that degradation simulation has to be performed only once for each single transistor device (PMOS and NMOS respectively). Their corresponding sensitivity values are saved in a database. This sensitivity value universally serves as a measure for circuit performance degradation and helps to find operating points of a transistor, which are less susceptible to aging than the nominal ones. The resulting circuit is sized for an optimized degradation behavior.

In order to observe reliability on system-level and speed up simulation, the behavior of a system's component is modeled in an analog hardware description language in dependence of age and process parameters. A method using design of experiments to generate models from distinct simulation points is presented. All methods are verified on circuit examples on a 150 nm and 350 nm technology node utilizing RelXpert aging models.

2. Aging-aware sizing of transistors

To design circuits with high lifetimes, counter measures have to be taken to harden a device against aging mechanisms. Structural change in the circuit topology which does not affect the main characteristics is one possibility to harden a circuit. For analog circuits such as amplifiers, which are widely used in many integrated systems, the impact of age-dependent degradation on certain output performance characteristics can be shown and investigated.

MOS only reference (MOR) and beta matching reference (BMR) circuits as shown in Fig. 1 are used for biasing a Folded Cascode OTA in combination with either wide swing (WS) or single MOS (SM) current mirror configuration integrated in the amplifier. Fig. 2 depicts the percentage shifts of the DC-Gain and the Gain-bandwith (GBW) of the Folded Cascode OTA with the different voltage reference circuits for a degradation time of $t_{age} = 1000$ days. It can be shown that the degradation is dependent on the used bias circuit. By choosing the bias circuit which results in a minimal shift (indicated in light grey), a degradation-aware design can be found.

Apart from this structural design approach, operating point dependent methods can be used to develop aging-aware circuits as described in the following. This method does not require a change of the overall structure of the circuit, but focuses on the resizing of transistors for an optimum performance in regard to aging. In order to fulfill certain functionalities and specifications, the dimensions of the individual transistors of a circuit have to be chosen accordingly. The operating point is an important criterion which includes all essential small signal parameters that sufficiently describe circuits like amplifiers and comparators. An operating point is described by fixed values of the drain current I_D and transistor dimensions $^W/_L$. This allows a straight forward hand-calculation of many design aspects

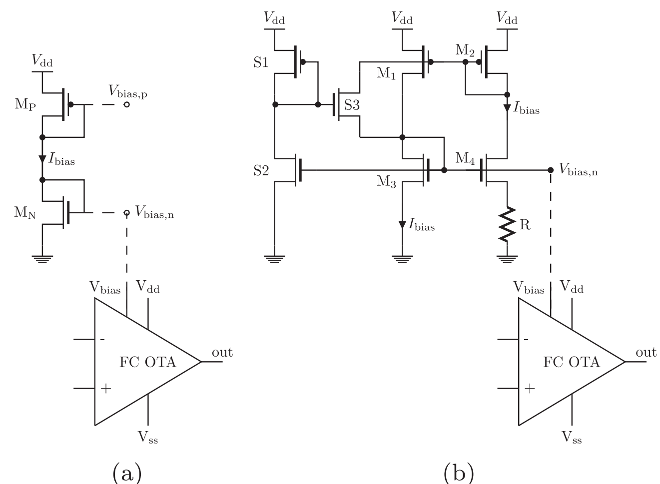

Fig. 1. Schematic view of different biasing circuits for Folded Cascode OTA. (a) MOS only reference. (b) Beta matching reference.

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