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Study of total ionizing dose induced read bit errors in magneto-resistive random access memory

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ABSTRACT

This paper presents the Co-60 irradiation results for a 16 Mb Magneto-resistive Random Access Memory (MRAM). Read bit errors were observed during Total Ionizing Dose (TID) testing. We have investigated their physical mechanisms and proposed a resistance drift model of the access transistor in 1M1T (a magnetic tunnel junction and a transistor) storage structure to understand the phenomenon. Read operations have been simulated by HSPICE simulator with the magnetic tunnel junction (MTJ) compact model. The simulation results reveal that the resistance shift of access transistors has a great impact on read bit errors in MRAM. The experimental data and analysis in this work can be used to harden MRAM designs targeting space-borne applications.

1. Introduction

In the space radiation environment, there are a variety of extremely energetic particles, such as protons, electrons, and heavy ions [1–2]. Ion strikes may alter the insulator's properties in metal-oxide-semiconductor field-effect transistor (MOSFET) and consequently induce radiation effects. These effects have been identified as the major reliability issues for microelectronic systems. As total ionizing dose effects pose a long-term impact on electronic devices, it is not surprising that these effects and their mitigation techniques for devices targeting harsh radiation environments [3] have been studied by the community.

A majority of modern system on chips (SOCs) are constructed with memories and they may occupy up to 95% of the overall die area [4]. With wide applications of SOCs in spacecrafts and satellites, space-grade electronic systems call for novel non-volatile memory devices featuring both higher density and reliability [5–7]. Magneto-resistive Random Access Memory is believed to be one of the promising candidates. This is because it has unique advantage compared to conventional memories (e.g., SRAM and FLASH) in terms of speed, integration density, unlimited endurance, less power consumption [8–10], and inherent immunity to radiation strikes [11–13]. Each MRAM bit-cell is composed of an access transistor and a MTJ (Magnetic Tunnel Junction). The MTJ device has a free ferromagnetic layer and a pinned ferromagnetic layer separated by a thin insulator layer. Due to the parallel or anti-parallel magnetizations of these two ferromagnetic layers, MTJs exhibit two stable resistance states, low or high [14].

Previous TID testing results have demonstrated that neither the electrical nor the magnetic properties of MTJs exhibited errors induced by radiation strikes [12,13]. However, during our experiments, we observed read bit errors in MRAM chips after total dose reached a certain threshold value. To our best knowledge, there are no complete or reasonable explanations w.r.t. how TID affects MRAM storage cells and consequently leads to read bit errors.

In this work, we investigate TID effects on MRAM devices induced by Cobalt-60. Main electrical parameters of MRAM are monitored and read bit errors as a function of total dose are investigated. We also present a resistance drift model to understand the read bit error's phenomenon induced by TID radiation.

2. DUT and test procedure

The Device Under Test (DUT) in our work is a commercial MRAM device-MR4A08B, the vendor of which is Everspin Corporation. It has 16 Mb 1M1T (1 MTJ and 1 access transistor) storage cells. The access transistor features gate oxide of 2.8-nm thickness and W/L = 0.8 μm/0.18 μm. The shallow trench isolation (STI) is introduced for electrical isolation with the depth of approximately 380 nm. The MRAM devices feature 3.3 V power supply, 8 bits wordwidth, 9 mA AC standby current,

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and SRAM-compatible 35 ns access time with unlimited endurance. MR4A08B utilizes 44-lead plastic TSOP package.

The TID radiation experiments were performed at the Department of Technical Physics of Peking University with a cobalt-60 radiation source at a dose rate of 50 rad(Si)/s. Electrical measurements were conducted at 0, 20, 30, 40, 45, 50, 55, 65, 75 krad(Si) respectively. During TID irradiation, the DUTs were biased at the worst-case condition. The enable pins of MRAM (/E, /W, /G) were pulled up, address and data pins were connected to 3.3 V. All the DUTs were initially programmed with the checkerboard pattern (i.e., 55H) and read back between each dose step. Subsequently, electrical parameters were measured. Finally, the pattern of all-0(all-1) was tested and March_6N test were performed. March_6N is a memory test approach designed to uncover a variety of faults. It is formally written as:

$$\{\uparrow(w55H);\uparrow(r55H,wAAH);\downarrow(rAAH,w55H);\uparrow(r55H)\}$$

The sequences are:

write 55 with ascending order of address;
read 55 and write AA with ascending order;
read AA and write 55 with descending order;
finally read 55 with ascending order.

This test procedure was repeated at each irradiation step until total dose was accumulated up to 75 krad(Si). This is in accordance with the specifications in MIL-STD-883D Test Method 1019.4 — start electrical characterization within 1 h after exposure and finish within 2 h before the next run. All the parameters of the DUTs were measured with the Verigy 93000 SOC test system. After the final irradiation step, the DUTs were annealed at room temperature up to 120 h with pins electrically floating.

3. Experimental results and discussion

3.1. Read bit errors and DC parameters versus TID

Below 55 krad(Si) dose level, all the DUTs remained fully functional. After the dose was accumulated to 65 krad(Si), all the devices started to read out erroneous data when the initial data pattern was 55H. When read bit errors were detected, error types and their corresponding logic address were logged. Error distribution differs from each DUT and random logic address were observed. The read bit error counts and types are summarized in Table 1. '1 → 0' means the bit is initially 1 and then flips to 0. In fact, DUTs 1 through 3 observed 1, 5169 and 30 bit errors, respectively.

When the accumulated total dose surpassed the threshold value, read error bits started to grow exponentially [14,15]. Due to process variation, these DUTs exhibited different TID radiation threshold values around 65 krad(Si). 65 krad(Si) may be higher than the TID threshold of DUT2, and thus, DUT2 showed more bit errors compared with other DUTs.

Table 2 compiles the number of multiple upset per byte for each operation of reading '55H'. Fig. 1 shows the standby current I_{SB} as a function of the irradiation dose and annealing time. As can be seen, I_{SB} rises sharply starting 75 krad(Si) and surpasses the specification limit of 9 mA. The other DC parameters show the same variation trend as standby current.

Table 1
Read error types and count caused by TID effects in reading initial '55H' pattern.

Samples	Total dose	Error count	Error types	
			0 ⟶ 1	1 ⟶ 0
DUT1	65 krad(Si)	1	0	1
DUT2		5169	1060	4109
DUT3		30	11	19
DUT1	75 krad(Si)	3319	1233	2086
DUT2		11,864	1099	10,765
DUT3		9415	1059	8356

Table 2
Multiple upset per byte caused by ionizing irradiation.

Sample	Total dose	Total bytes	Multiple upset per byte			
			2 bits	3 bits	4 bits	5 bits
DUT1	65 krad(Si)	0	0	0	0	0
DUT2		112	110	2	0	0
DUT3		6	2	1	2	1
DUT1	75 krad(Si)	76	70	5	1	0
DUT2		1764	1251	396	114	3
DUT3		1022	917	104	1	0

3.2. The resistance drift of access transistor during TID irradiation

Fig. 2 displays the cross-sectional TEM (Transmission Electron Microscope) view of the 1M1T storage cell. The memory is fabricated on a 180 nm CMOS process with 5 metal layers and the MTJ is created during backend process steps between the last two metallization layers. As peripheral circuits have been demonstrated to be functional throughout our experiments, we have therefore studied TID effects on the access transistor in 1M1T storage cell.

Even though the MTJ itself is insensitive to TID effects, the radiation source may still degrade the performance of access transistors. In the structure of 1M1T, the gate oxide thickness of the access transistor is 2.8 nm and is believed to be less sensitive to TID exposure. This is because reduction in gate oxide thickness essentially eliminates radiation-induced performance degradation, as discussed in previous results [16–18]. By contrast, the STI oxide thickness is 380 nm and does not scale down correspondingly, TID radiation will induce significant charge trapping in STI region [19,20].

Prior to irradiation, the channel resistance of access transistor [21] is calculated as

$$R_{mos} = \frac{L}{W}\cdot\frac{1}{u_n C_{ox}(V_{gs}-V_t)} \tag{1}$$

where L and W represent the length and width of transistor respectively, C_{ox} is gate oxide capacitance per unit area,V_{gs} is the voltage between gate and source region,V_t is the threshold voltage, u_n is carrier mobility. The linear channel resistance is given in Function (1), as can be seen, small changes in carrier mobility or threshold voltage of access transistor would lead to the obvious variations of channel resistance.

Fig. 3 shows the structure of STI parasitic transistor where the trench oxide serves as the thick gate oxide. In a 1M1T storage cell, the access transistor is composed of a main transistor and two parasitic edge transistors. The threshold voltage shift of the STI parasitic transistor induced by TID effects is given by:

$$\Delta V_t = \Delta V_{ot} + \Delta V_{it} = -\frac{q(\Delta N_{ot}+\Delta N_{it})t_{OX}}{\varepsilon_0\varepsilon_{OX}} \tag{2}$$

where ΔV_{ot} and ΔV_{it} are the voltage shifts caused by oxide trapped charge and interface trapped charge respectively. ΔN_{ot} is the oxide trapped charge density, ΔN_{it} means the interface trapped charge density, and t_{OX} is the thickness of gate oxide.

After TID irradiation, the channel resistance of access transistor R'_{mos} becomes:

$$R'_{mos} = \frac{L}{W+\Delta w}\frac{1+a_{it}\Delta N_{it}}{u_0 C_{ox}}\frac{1}{\left[V_{gs}-V_t+\frac{q}{C_{ox}}(\Delta N_{ot}+\Delta N_{it})\right]} \tag{3}$$