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Efficient reliability evaluation methodologies for combinational circuits

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ABSTRACT

Reliability evaluation methodologies have become important in circuit design. In this paper, we focus on the probabilistic transfer matrix (PTM), which has proven to be a gate-level approach for accurately assess the reliability of a combinational circuit with penalty in simulation runtime and memory usage. In order to improve its efficiency, several methodologies based on traditional PTM are proposed. A general tool is developed to calculate the reliability of a circuit with efficient computation methods based on an optimized PTM (denoted as ECPTM), which achieves runtime and memory usage improvement. Experiments demonstrate how the proposed simulation framework, combined with traditional PTM method, can provide significant reduction in computation runtime and memory usage with different benchmark circuits.

1. Introduction

CMOS technology scaling according to Moore's law drives the need for high reliability in integrated circuits (ICs) [1]. With the dimension shrinking to nanometer regime, transistors are more prone to reliability issues such as single event transients (SET) [2], [3], [4], process variations [5] and aging effects [6]. Moreover, in order to keep the energy consumption constant or at a low level, the supply voltage should shrink linearly with the dimension, which leads to an increase in noise that may cause errors [7], [8].

The soft errors occur at the storage cells (e.g., latches), especially in aerospace applications. The α-particles, cosmic rays and atmospheric neutrons existing in the earth atmosphere are able to generate current pulse which may induce soft error if this current pulse is sufficient enough in amplitude and time duration [2]. It was generally accepted that current pulses cannot cause soft errors in logic circuits because of the existence of masking effects: logical masking, electrical masking and latching-window masking [9]. However, with the transistor dimension scaling down, the drastic reduction of noise margin, the much higher operating frequency and the lower threshold voltage have improved the probability of a current pulse captured by a latch and consequentially introduce soft error in logic circuits.

In order to design reliable ICs, probability transfer matrix (PTM) is applied to reliability evaluation of combinational circuits [10]. At gate level, the conditional probability of every output vector given a particular input vector can be obtained accurately. The main drawbacks of PTM are the excessive usage of memory and computational complexity required to manipulate matrices. Several methods have been proposed to optimize simulation time and memory usage in PTM. In [11], an approach to compress the memory space usage is proposed based on algebraic decision diagrams, but only for square matrices. Another improvement method is described in [12], which can reduce the memory usage and time consumption by eliminating some useless but expensive inter-data.

This work presents a novel framework that leads to drastic reduction in computation runtime and memory usage. The rest of paper is organized as follows. Section 2 recalls PTM basics. The proposed methodologies are presented in Section 3. Section 4 describes the general tool developed for reliability estimation of a circuit. Experimental results are shown in Section 5. Finally, conclusions are outlined in Section 6.

2. Probabilistic transfer matrix

Assume a logic circuit with input x and output y, where $x \in \{x_0, x_1, \cdots, x_i, \cdots, x_{2^m-1}\}$ and $y \in \{y_0, y_1, \cdots, y_j, \cdots, y_{2^n-1}\}$. The corresponding PTM, denoted M, has $2^m \times 2^n$ elements and each (i,j) element is the probability of getting output $y = y_j$ given the occurrence of input $x = x_i$, noted $p(j|i)$. In the case of an ideal (i.e. fault free) circuit, the PTM contains only zeros and ones and is named ITM (Ideal Transfer Matrix). Fig. 1 shows the PTM for an NAND logic gate with error probability equals to $1-q$, where q represents the probability of getting a correct output. It should be noted that ITM is defined for $q = 1$.

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The reliability of a circuit is directly extracted from the respective *PTM* and *ITM*, according to Eq. (1), where $p(i)$ denotes the probability that input x is x_i.

$$R = \sum_{ITM(i,j)=1} p(j|i)p(i) \tag{1}$$

The expression above gives the sum of probabilities corresponding to correct outputs. That is, the element in position (i,j) of *PTM* matrix contributes to the sum only if the respective (i,j) element of the *ITM* has a value 1. Since the PTM gives the exact probabilities of getting correct outputs, the above expression provides accurate reliability assessment.

To calculate PTM of a whole circuit, PTMs of its basic gates are combined by using matrix operations, depending on the manner as they are assembled. Let be the gates G_1 G_2, with their respective PTMs M_{G_1} and M_{G_2}. If G_1 and G_2 are connected in series, the global PTM M_T can be achieved by $M_{G_1} \cdot M_{G_2}$. If G_1 and G_2 are connected in parallel, the global PTM M_T can be calculated with tensor product, $\otimes$. Thus, the resulting global PTM is $M_{G_1} \otimes M_{G_2}$.

Assuming the input of G_k is a m_k-bits vector while its output is a n_k-bits vector. The PTM of a logic gate G_k, noted M_{G_k}, contains $2^{m_k} \times 2^{n_k} = 2^{m_k + n_k}$ elements. The computational complexity C_T related to obtaining the resulting matrix M_T can be expressed in terms of the cost and the number of multiplications and additions between elements of the basic involved matrices M_{G_k}. If G_1 and G_2 are connected in series, n_1 must be equals to m_2. Each element in the resulting matrix can be expressed as:

$$Z(i,j) = \sum_{u=0}^{2^{n_1}-1} M_1(i,u) \times M_2(u,j) \tag{2}$$

The matrix M_T contains $2^{m_1} \times 2^{n_2}$ elements. The total number of arithmetic operations required to obtain it is given by Eq. (3), where $C_\otimes$ denotes the complexity of a multiplication while $C_\oplus$ denotes the complexity of an addition. This leads to the complexity estimation as $\mathcal{O}(2^{m_1+n_2+n_1})$.

$$C_Z = 2^{m_1} \times 2^{n_2} \left[2^{n_1} \times C_\otimes + (2^{n_1} - 1) \times C_\oplus\right] \tag{3}$$

In the case of gates connected in parallel, each element in the resulting matrix can be expressed as Eq. (4), where $u = i \bmod m_2$ and $v = j \bmod n_2$.

$$P(i,j) = M_1(\lfloor i/m_2 \rfloor + 1, \lfloor j/n_2 \rfloor + 1) \times M_2(u,v) \tag{4}$$

The matrix M_T contains $2^{m_1+m_2} \times 2^{n_1+n_2}$ elements. The total number of arithmetic operations required to obtain it is given by Eq. (5), where $C_\otimes$ denotes the complexity of a multiplication while $C_\oplus$ denotes the complexity of an addition. Similarly to gates in series, the complexity related to gates connected in parallel is $\mathcal{O}(2^{m_1+m_2+n_1+n_2})$.

$$C_P = 2^{m_1+m_2} \times 2^{n_1+n_2} \times C_\otimes \tag{5}$$

3. Efficient computation methods based on PTM (ECPTM)

Let be a general combinational circuit as shown in Fig. 2. To calculate the reliability of such a circuit as defined in Eq. (1), the circuit PTM calculation is required. To calculate the PTM of a complex circuit including several gates in series and in parallel, the basic idea is to divide it as a cascade of W sub circuits or levels (see Fig. 2a). Each level l has a PTM matrix, noted $P_{K_l}^{\ l}$, that results of tensor products applied to PTMs of all K_l parallel B_k^l logic blocks existing in level l (see Fig. 2b).

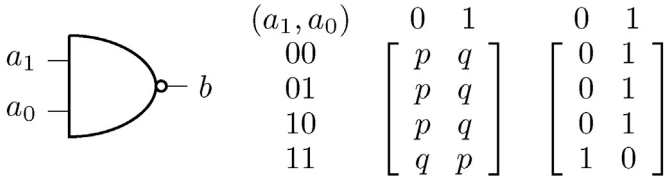

Fig. 1. Logic gate NAND with its PTM and ITM.

3.1. PTM calculation of complex circuits

The global PTM, noted Z_W, is given by progressive calculation of inner products of the W level matrices $P_{K_l}^{\ l}$ as below, where Z_l corresponds to the PTM for the cascade of first l levels:

$$\begin{aligned}
Z_2 &= P_{K_1}^1 \cdot P_{K_2}^2 \\
Z_3 &= \left(P_{K_1}^1 \cdot P_{K_2}^2\right) \cdot P_{K_3}^3 = Z_2 \cdot P_{K_3}^3 \\
Z_4 &= \left(\left(P_{K_1}^1 \cdot P_{K_2}^2\right) \cdot P_{K_3}^3\right) \cdot P_{K_4}^4 = Z_3 \cdot P_{K_4}^4 \\
&\vdots = \vdots \\
Z_W &= \left(\cdots\left(\left(P_{K_1}^1 \cdot P_{K_2}^2\right) \cdot P_{K_3}^3\right)\cdots\right) \cdot P_{K_W}^W = Z_{W-1} \cdot P_{K_W}^W
\end{aligned}$$

A new PTM Z_l is obtained at each step.

Each matrix Z_l has a number of elements which depend on the number of rows in the first level (that is, $P_{K_1}^{\ 1}$) and the number of columns in the matrix of level l (that is, $P_{K_l}^{\ l}$). The number of rows in $P_{K_l}^{\ l}$ comes from the number m_k^l of rows in the basic matrices of level l, noted M_k^l. Hence, $r_l = \prod_1^{K_l} m_k^l$. Equivalently, the number of columns in $P_{K_l}^{\ l}$ is $c_l = \prod_1^{K_l} n_k^l$. The total number of elements to be calculated to get Z_l is given by (Eq. (6)) and the respective computational cost is given by (Eq. (7)), where r_l and c_l are the number of rows and columns in $P_{K_l}^{\ l}$.

$$N = \sum_{u=2}^{l} (r_1 \times c_u) \tag{6}$$

$$N = \sum_{u=2}^{l} (r_1 \times c_u)[c_{u-1} \times C_\otimes + (c_{u-1} - 1) \times C_\oplus] \tag{7}$$

It should be noted that when PTM computation is done solely in order to assess reliability as given in Eq. (1), only a subset of elements $Z_K(i,j)$ in matrix Z_K are required. Actually, they are those corresponding

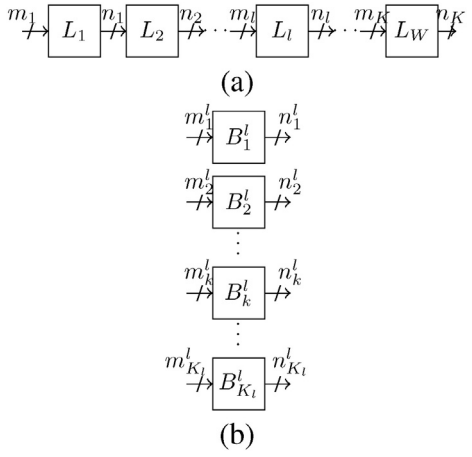

Fig. 2. (a) Cascade of W levels (or groups) of combinational blocks. (b) Detail of the parallel sub-blocks in the *lth* level.

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