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A process-variation-resilient methodology of circuit design by using asymmetrical forward body bias in 28 nm FDSOI

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ABSTRACT

Due to the process variation, Spin Transfer Torque Magnetic Tunnel Junction (STT-MTJ) faces great challenges in fabrication process. Meanwhile, its neighbor CMOS is also influenced by significant process variation with the continuous technology scaling down. Both of the two effects lead to degraded performance of hybrid MTJ/CMOS circuit. This paper proposes a methodology to alleviate the impact of process variation on the performance of MTJ based applications. The methodology is presented by carrying out a novel design of non-volatile flip-flop (NVFF) using asymmetrical forward body bias (FBB) in fully depleted silicon on insulator (FDSOI). Simulation results show that the sensing errors have been almost removed by this method with the minimum size of circuit. In addition, the thermal robustness of this circuit has also been dramatically improved.

1. Introduction

Spin transfer torque magnetic random access memory (STT-MRAM) is a promising memory candidate in the future embedded systems owing to its high energy efficiency, fast access speed, infinite endurance and great scalability [1,2]. In the past years, STT-MRAM has been explored for data storage and high-performance computing as an embedded non-volatile working memory [2,3]. Recently, it has shown great potential in emerging ultra-low standby-power connectivity systems such as wearable objects, IoT (Internet-of-Things) and secure elements [4].

However, as an essential element of STT-MRAM, magnetic tunnel junction (MTJ) suffers from significant process variations [5]. Many methods have been used to improve the device performance and uniformity, such as optimizing device design and process control [6]. Nonetheless, with continuous scaling down of process technology, the impact of process imperfection due to lithography and inherent film variations (i.e., surface roughness, material inhomogeneity, etc.) becomes more and more severe. Consequently, MTJ static and dynamic behavior are significantly influenced, leading to a number of failure issues in write and read operations, and these functional errors are uncorrected after fabrication [7]. Thus, it is important to enhance the reliability of the circuit by taking into account the process variations of MTJ at the early design phase.

Easy integration into conventional CMOS circuits is the trump of MTJ which makes it outstanding among all the emerging devices in semiconductor applications. Nevertheless, the neighbor transistors are also deeply affected by process variations. This further deteriorates the variability tolerance of hybrid MTJ/CMOS circuits.

Recently, transistors with fully depleted silicon on insulator (FDSOI) technology have shown high immunity to threshold voltage variability [8]. Compared with bulk CMOS device, FDSOI transistor enables both computing at a very high frequency and better performance with ultra-low voltage operations. Thus, circuit function can be guaranteed with maximum energy efficiency [9]. The forward/reverse body bias (FBB/RBB) allows the designers to dynamically adjust the threshold voltage (V_{th}) of the transistors over a wide range [10]. In addition, with a slight increase in transistor gate length, leakage power can be effectively reduced (poly bias technique). Fig. 1 displays the cross-section view of hybrid MTJ/CMOS circuit as well as the typical structure and switching mechanism of MTJ [11].

This work proposes a novel methodology of process variation aware design by using asymmetrical forward body bias in a non-volatile flip-flop (NVFF). The circuit is implemented by using 28 nm FD-SOI technology and a compact model of MTJ. Reliability issues of process variations, stochastic switching, temperature fluctuation and dielectric breakdown phenomenon are included in this model [12]. It has been integrated in the design of hybrid MTJ/FDSOI circuits and systems to analyze and optimize operation speed, area and energy performance [13].

The rest of the paper is organized as follows. Section 2 introduces the compact model of MTJ, which includes process variations. In Section 3, the performance characteristics of FDSOI are presented in details.

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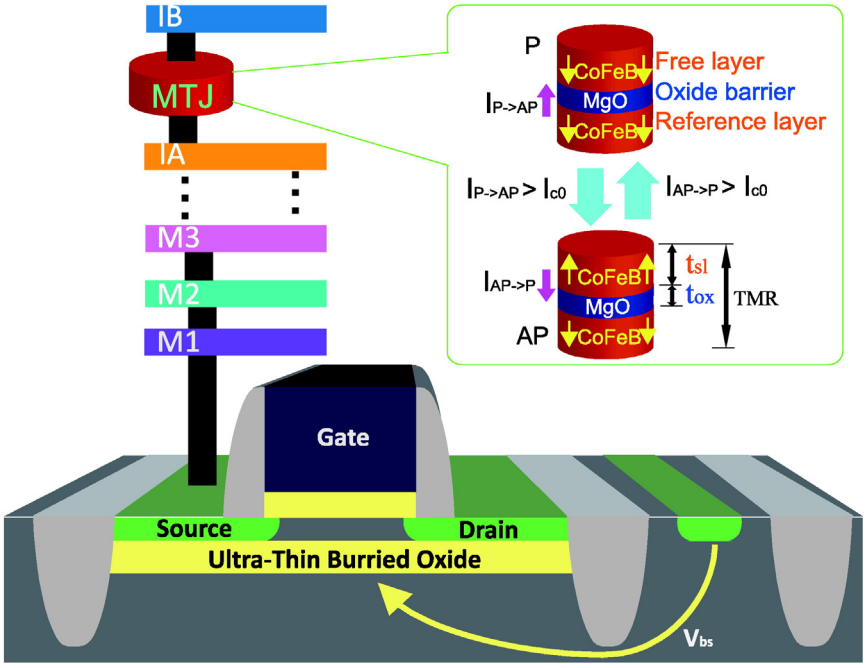

Fig. 1. MTJ consists of two ferromagnetic (FM) layers separated by an oxide barrier. The nanopillar resistance (R_p, R_{ap}) depends on the relative magnetization of the two FM layers (Parallel (P) or Anti-Parallel (AP)) [1]. The resistance difference is characterized by Tunnel Magnetoresistance Ratio $TMR = (R_{ap} - R_p)/R_p$. According to the STT mechanism, MTJ changes between two states when a bidirectional current I higher than the critical current I_{c0} flows through the device. The main process parameters which have impact on MTJ performance are indicated above. MTJ integration with FDSOI transistors in the metal stack: MTJ is always deposited at the highest level of metal; V_{bs} is the body bias of transistor.

Section 4 focuses on the circuit design of NVFF and the detailed simulation results of reliability analysis, followed by the conclusion.

2. Compact model of MTJ including process variations effect

Our previous work has validated a compact model of perpendicular magnetic anisotropy (PMA) STT-MTJ [14]. This model includes the static and dynamic characteristics of PMA-MTJ device. The static model concerns the calculation of MTJ resistance (R_p, R_{ap}) and critical switching current I_{c0}:

$$R_p = \frac{t_{ox}}{\left(F \cdot \overline{\varphi}^{1/2} \cdot Area\right)} \cdot \exp\left(coef \cdot t_{ox} \cdot \overline{\varphi}^{1/2}\right) \quad (1)$$

$$I_{c0} = \alpha \frac{\gamma e}{\mu_B g}(\mu_0 M_s) H_K V = \frac{2\alpha\gamma e}{\mu_B g} E \quad (2)$$

where $\overline{\varphi}$ is the average potential barrier height of MgO (0.4 eV), *coef* is a fitting parameter and F is another fitting parameter depending on the material composition of the three thin layers [15]. E is the barrier energy, μ_0 is the permeability of free space, M_s is the saturation magnetization, H_K is the effective anisotropy field, V is the volume of the free layer, α is the damping constant, γ the gyromagnetic ratio, e is the elementary charge, μ_B is the Bohr magneton, and $g = \sqrt{TMR(TMR+2)}/2(TMR+1)$ is the spin polarization efficiency factor.

The dynamic model involves emulating the real time switching behavior of MTJ under voltage or current pulse. Depending on the magnitude of switching current, the switching behavior of MTJ can be divided into two regimes [16]: Sun model ($I > I_{c0}$) and Neel-brown model ($I < 0.8I_{c0}$). The switching delay can be calculated as follows [17,18]:

$$\tau = \tau_0 \exp\left(\frac{E}{k_B T}\left(1 - \frac{I}{I_{c0}}\right)\right) \quad (I<0.8I_{c0}) \quad (3)$$

$$\frac{1}{\langle\tau\rangle} = \left[\frac{2}{C + \ln\left(\frac{\pi^2\Delta}{4}\right)}\right] \frac{\mu_B P_{ref}}{e m_m (1 + P_{ref} P_{free})} (I - I_{c0}) \quad (I>I_{c0}) \quad (4)$$

where τ_0 is the attempt period, k_B is the Boltzmann constant, $C \approx 0.577$ is the Euler's constant, m_m is the magnetization moment and P is the tunneling spin polarizations.

The equations presented above show that the following three parameters are critical to static and dynamic behavior of MTJ: thickness of oxide barrier t_{ox}, thickness of switching layer t_{sl}, and the tunnel magnetoresistance ratio TMR. The parametric variations are assumed as normal distribution with a specification of σ/μ (σ is the standard deviation and μ is the mean value of normal distribution). The process variation is integrated into the model by using random functions in Verilog-A language [12]. The users are free to reconfigure the simulation conditions by choosing different types of statistical distributions (uniform or normal) for device parameters (t_{sl}, t_{ox} and TMR).

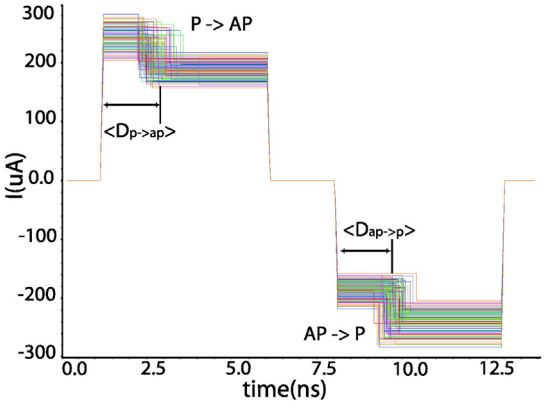

Fig. 2. 1000 complete writing operation Monte-Carlo simulations with the parameters variation.

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