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Impact of resistive paths on NVM array reliability: Application to Flash & ReRAM memories

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ABSTRACT

In memory technology, size reduction induces consequences in terms of reliability, including an increase in the line resistances and a voltage drop along the line during memory operation. This problem can occur in Flash products during sector erase mode, and in resistive RAM (ReRAM) during forming, reset or word-reading modes.
In this paper we apply a simple resistive model to determine the wordline (or bitline) length of a Flash memory (and thus to optimize the Flash memory array's size) or the word length of a ReRAM, according to specific reliability criteria: the threshold voltage drop of cells along a line in a Flash memory sector, or the resistance variation of the cells in a ReRAM word.
For the technologies considered in this paper, on the one hand we demonstrate a maximal threshold voltage drop of 2 V for a 4 Gbit Flash array and we provide design recommendations, and on the other hand we demonstrate that a maximal word length of 32 bits for ReRAM can be achievable in a ReRAM matrix. The presented methodology can easily be extended to any memory technology.

1. Introduction

At sub 45 nm feature, size reduction increases the resistivity of interconnects, inducing a voltage decrease along the memory matrix lines which can cause severe reliability issues. This problem is often solved in Flash memory with additional reconnections, which consume cell area and increase the cost-per-bit [1]. For new emerging memory technologies such as ReRAM, the data is stored as two resistance states of the resistive switching device. This feature makes these memories sensitive to resistive paths. In this context, effect of wordline (WL) or bitline (BL) scaling on the performance and reliability of ReRAM memory array is under investigation [2]. Indeed, in case of Flash sector or ReRAM word selections, a voltage drop occurs along the line, which can be critical during memory programming or reading when multiple cells are simultaneously selected. This voltage drop prevents cells from operating properly (especially cells located at the end of the lines). This is the case in the Flash memory during the erasing of a whole sector [1]. It is also the case in ReRAM memory during FORMING or RESET operations when cells are selected by words [3].

2. Line modeling

In this part, we want to evaluate the real output voltage value relative to the applied voltage at the line entrance.

A resistive model [4] based on the line resistance R_A and on the memory cell equivalent resistance R_C shows the decrease of the output voltage V_{OUT} at the end of the line. Let us then consider a memory line constituted of N cells, represented in this model by their equivalent resistance R_C (Fig. 1).

2.1. Iterative model

2.1.1. Iterative calculation of the output voltage of a line constituted by N cells

With a low resistance, R_C, the decrease will appear for a low number of cells in the line, N. Then the calculation can be conducted with an iterative method and gives the exact result for the equivalent schematic (Fig. 1) according to the Thevenin theorem:

$$V_{OUT,N} = \left(V_{OUT,N-1} \cdot R_C\right)/\left(R_C + R_{O,N}\right) \quad (1)$$

where $R_{O,N} = R_A + (R_C // R_{O,N-1})$. The initial conditions for $N = 1$ are $R_{O,N=1} = R_A$ and $V_{OUT,N-1=0} = V_{IN}$. Fig. 2 shows the result for a memory line of N cells.

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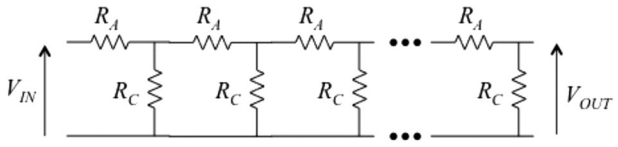

Fig. 1. Equivalent schematic of the memory line.

2.1.2. Iterative calculation of the entrance resistance of a line constituted by N cells

The calculation can be conducted with an iterative method:

$$R_{IN,N} = R_A + (R_C // R_{IN,N-1}) \tag{2}$$

The initial condition for $N=1$ is $R_{IN,N=1} = R_A + R_C$. Fig. 3 shows the result for a memory line of N cells.

2.1.3. Calculating the voltage distribution inside the line constituted by N cells

It is very important to notice that the output voltage versus cells number is not representative of the voltage distribution inside a memory line.

We calculate the voltage of a given cell (numbered n) inside a memory line constituted of N cells with the following equation:

$$V_{N,n} = V_{N,n+1} \cdot (R_A + R_{L,N-n+1})/R_{L,N-n+1} \tag{3}$$

where $R_{L,N-n} = R_C//(R_A + R_{L,N-n+1})$.

The calculation starts at the end of the line, with $n=N$: the initial conditions are $R_{L,N-n} = R_{L,0} = R_C$ and $V_{N,N} = V_{OUT,N}$. Fig. 4 shows the voltage distribution in a memory line constituted of $N = 30$ cells, compared with the output voltage versus cells number, N.

With a high resistance, R_C, the voltage decrease appears for a high number of cells in the line, N. Then, the iterative calculation duration is very long. A matrix calculation allows finding an explicit expression of the output voltage and of the entrance resistance.

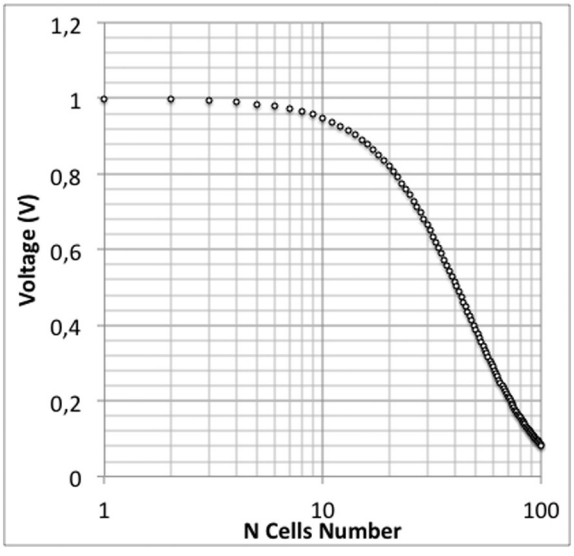

Fig. 2. Iterative calculation of the output voltage of a line constituted of N cells, with $R_A = 1\ \Omega$, $R_C = 1\ k\Omega$ and $V_{IN} = 1$ V.

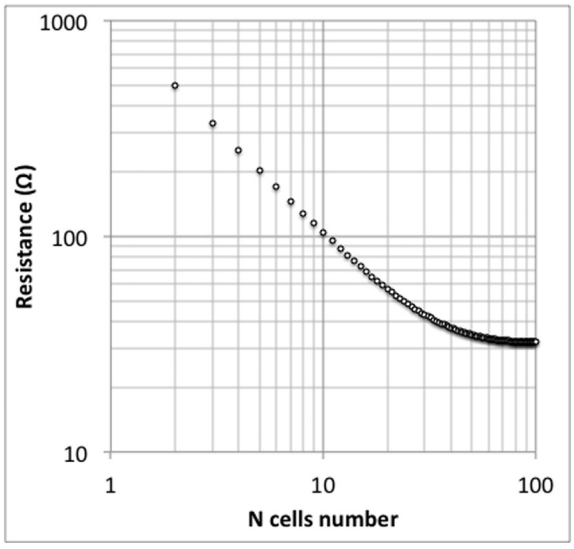

Fig. 3. Iterative calculation of the entrance resistance of a memory line constituted of N cells, with $R_A = 1\ \Omega$, $R_C = 1\ k\Omega$ and $V_{IN} = 1$ V.

2.2. Explicit model

Let us consider the matrix of a quadripole (1: entrance; 2: output):

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{bmatrix} K_{11} & K_{12} \\ K_{21} & K_{22} \end{bmatrix} \cdot \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} \tag{4}$$

The matrix calculation is interesting because it gives the transmittance $H = (V_2/V_1)_{I_2=0} = 1/K_{11}$, the entrance resistance $R_{IN} = (V_1/I_1)_{I_2=0} = K_{11}/K_{21}$ and the output resistance $R_{OUT} = (V_2/I_2)_{V_1=0} = K_{12}/K_{11}$.

2.2.1. Matrix calculation

For a memory line constituted of N cells, with a line resistance, R_A, and a cell equivalent resistance, R_C, and defining $x = R_A/R_C$ we get:

$$\begin{bmatrix} K_{11} & K_{12} \\ K_{21} & K_{22} \end{bmatrix} = \begin{bmatrix} P_{1,N}(x) & R_A \cdot P_{2,N}(x) \\ P_{2,N}(x)/R_C & P_{1,N-1}(x) \end{bmatrix} \tag{5}$$

with:

$$P_{1,N}(x) = 1 + \sum_{k=1}^{N} a_{k,N} \cdot x^k \tag{6}$$

$$P_{2,N}(x) = N + \sum_{k=1}^{N} b_{k,N} \cdot x^k \tag{7}$$

The 1st order ($k=1$) coefficients can be expressed (with $a_{1,1}=1$ and $b_{1,1}=0$) by:

$$a_{1,N} = N^2 - a_{1,N-1} \tag{8}$$

$$b_{1,N} = b_{1,N-1} + a_{1,N-1} \tag{9}$$

And when N is even ($N=2n$ with $n \in \mathbb{N}$) or odd ($N=2n-1$) we have the explicit expression [4]:

$$a_{1,N=2n} = 2n^2 + n \tag{10}$$

$$a_{1,N=2n-1} = 2n^2 - n \tag{11}$$

2.2.2. Output voltage of a line constituted by N cells

At zero order ($k=0$; $P_{1,N}(x)=1$ and $P_{2,N}(x)=N$) we have $V_{OUT,N} = V_{IN}$ whatever N.

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