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Instability of oxide thin film transistor under electrical–mechanical hybrid stress for foldable display

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ABSTRACT

Degradation mechanism of foldable thin film transistors (TFTs) is investigated experimentally by electrical, mechanical and electrical–mechanical hybrid stress experiments. Mechanical and electrical stress environment was set for foldable TFTs and the degradation effect according to the applied stress is investigated and analyzed. Degradation mechanism model that can explain the defect generation is suggested to explain the result of electrical–mechanical hybrid stress experiment.

1. Introduction

Flexibility is the key issue for the next generation display. In advance of the current curved-shape display, next generation of the display can be bendable and foldable display. Among all types of transistors, amorphous indium–gallium–zinc oxide (a-IGZO) semiconductor is an attractive candidate due to its good electrical performance and possibility of fabrication at low temperatures (<300 °C) [1]. In addition, a-IGZO is reported as having the smallest variations of the electrical properties with strain [2]. For the realization of next generation of display, the stability of foldable thin film transistors (TFTs) after the mechanical stress should be confirmed. Several studies investigated that the extra stress, such as bias stress to the gate, causes degradation in the electrical characteristic of TFTs [3,4]. It is also known that continuous mechanical stress to thin film transistors causes the degradation in electrical performance of thin film transistor [5]. However, both electrical and mechanical stresses cannot be separated and should be considered simultaneously for the real usage in the foldable display. In this paper, the instability characteristic of foldable thin film transistor under electrical–mechanical hybrid stress is investigated and analyzed.

2. Experiment

2.1. Foldable TFTs

The tested foldable TFT fabricated as a conventional staggered bottom gate structure on the polyimide substrate is schematically shown in Fig. 1. The gate was fabricated with copper and molybedenum–titanium (MoTi) alloy. SiO_2 gate dielectric was deposited and amorphous indium–gallium–zinc-oxide (a-IGZO) layer was then deposited. The etch stopper layer was deposited on top of an active layer. The source and drain electrodes were fabricated by copper and MoTi alloy. Fabricated TFTs were detached by laser from the glass for the flexibility [6].

For the analysis of the electrical characteristic of TFTs, the current–voltage (I—V) characteristics of TFTs were measured using the Hewlett Packard 4145B parameter analyzer. The current–voltage characteristics were measured at the drain voltage of 10.1 V.

2.2. Experimental setup for static mechanical stress

Static mechanical stress was given to the TFTs using customized bending plate with 2.5-mm (2.5 R) bending radius. The direction of bending was outward with respect to the substrate (tensile) and parallel to the channel width as depicted in Fig. 1.

2.3. Experimental setup for hybrid stress

Three different environmental stress experiments on the TFT were proceeded independently including electrical stress with positive gate bias, mechanical stress and hybrid experiment of combining both electrical and mechanical stress in this work.

In the electrical stress experiment, 30 V of positive gate bias was given for 1000 s. During the electrical stress experiment, the electrical characteristic of TFT was measured at 0 s, 30 s, 100 s, 200 s, 500 s and 1000 s, respectively. Electrical characteristic was measured by the current–voltage (I—V) characteristic using the Hewlett Packard 4145B

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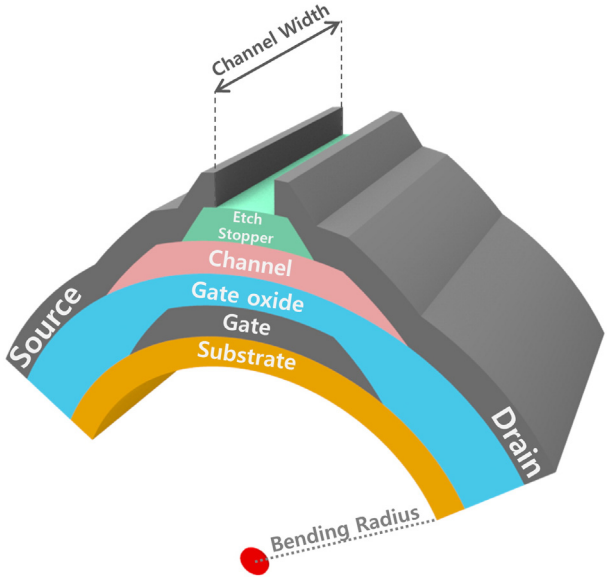

Fig. 1. Schematic structure of oxide TFT on the polyimide substrate under static mechanical stress.

parameter analyzer. The current–voltage characteristics were measured at the drain voltage of 10.1 V.

The static mechanical stress was applied for 168 h and the electrical characteristic of TFT was measured at 0 h (after stress), 24 h, 48 h, 72 h, 144 h and 168 h, respectively.

For the electrical and mechanical hybrid stress experiment, the same mechanical stress was given for 168 h and the electrical characteristic was measured the same as previous mechanical stress experiment. Simultaneously, 1000 s of gate bias stress was applied and the same measurement was proceeded after the electrical stress as depicted in Fig. 2.

2.4. Measurement

The change in electrical characteristics of TFTs was measured and variations of the turn-on voltage (V_{on}), the maximum drain current (I_{on}) and the field-effect mobility (μ_{eff}) were monitored [7]. All measurements were performed in the dark room.

The parameter of V_{on} was used in this paper instead of the threshold voltage (V_{th}) since there is an ambiguity standard on determining V_{th}. V_{on} was simply defined as the gate voltage at which the drain current increase begins in the current–voltage (I—V) characteristic [8].

Maximum drain current (I_{on}) was measured as the drain current value at gate voltage of 30 V.

The experimentally measured μ_{eff} was calculated as follows:

$$\mu_{eff} = \frac{G_m}{\left(\frac{W}{L}\right) C_i V_{DS}} \quad (1)$$

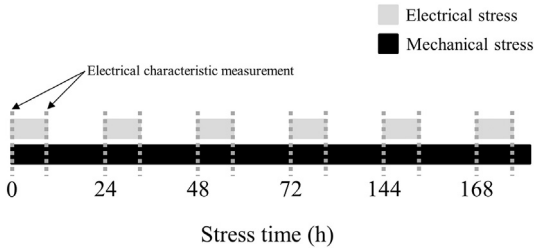

Fig. 2. Scheme of electrical and mechanical hybrid stress experiment.

where G_m is the transconductance, C_i is the gate capacitance per unit area, and V_{DS} is drain bias.

3. Result and discussion

The electrical characteristic of the static mechanical stress applied TFTs varies from the initial since electrical stress causes degradation [3].

The electrical stress caused degradation by V_{on} shift, I_{on} and μ_{eff} decrease as shown in Fig. 3(a). The degradation of electrical characteristic of TFTs can be explained by charge trapping in channel/dielectric interface or in the dielectric [9].

Fig. 3(b) shows the degradation of TFTs by static mechanical stress. Degradation induced by static mechanical stress is much larger than electrical stress induced degradation. This phenomenon can be explained by crack generation in gate insulator [10]. Generated cracks by mechanical stress can have a role as a defect site as shown in Fig. 4(b), which can trap electrons deeper than channel/dielectric interface layer. Moreover, trapped electrons in the dielectric layer can lead to the decrease in number of carriers in the channel which accelerates the degradation in mobility, on current and turn-on voltage [11].

In hybrid stress experiment, the tendency of degradation is similar with mechanical stress induced result including V_{on} shift, decrease in I_{on} and μ_{eff}. However, the amount of degradation in μ_{eff} is less than the result of mechanical stress experiment while degradation amount of I_{on} is similar. Decreased number of carrier caused by trapping at generated defect can explain the degradation in I_{on} and V_{on} as explained in mechanical stress experiment. However, less degradation in mobility can give us a clue for the location of generated defect. As shown in Fig. 5(b), repetitive positive electrical stress to the gate can refine the trapping sites in gate insulator uniformly and this can increase the effective mean free path of electrons. Therefore, longer mean free path of electron can increase the mobility of electron and relieve the amount of degradation compared to the result of mechanical stress without electrical stress [12].

4. Conclusion

The degradation mechanism of foldable thin film transistor was examined by comparing electrical, mechanical and electrical–mechanical hybrid stress experiments. The static mechanical stress induced defect generation in the dielectric layer. The degradation in V_{on}, I_{on} and μ_{eff} was caused by defect in the dielectric layer and this was explained by charge trapping at defect sites. Location of defect generated by mechanical stress was verified by mechanical and electrical hybrid experiment. By comparing mechanical stress and hybrid stress test, we found that defects are created in dielectric layer since there was a difference in the amount of degradation in mobility while other parameters remained similar. Decrease in number of carriers by trapping at generated defects is assumed as a main factor of degradation by mechanical stress. However, repetitive electrical stress can refine trapping sites in the dielectric layer and relieve the amount of mobility degradation by increasing mean free path of electron. Therefore, it can be concluded that defects by mechanical stress are created in dielectric layer and degradation in mobility by mechanical stress can be relieved by electrical stress. In addition, enhancing the reliability of foldable thin film transistor under mechanical stress should address improving mechanical reliability of dielectric layer and compensating the degradation in mobility is possible by an electrical method.

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