Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

FDSOI and Bulk CMOS SRAM Cell Resilience to Radiation Effects

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ARTICLE INFO

Article history:
Received 11 July 2016
Accepted 12 July 2016
Available online xxxx

Keywords:
FDSOI
Radiation
Heavy-ion
Single-event Effects
SET
SEU
Single-Event Transient
Single-Event Upset
TCAD

ABSTRACT

With shrinking dimensions and increased number of on-chip transistors radiation can provoke faults in integrated circuits even at sea level. This paper presents a comparison of fully depleted SOI (FDSOI) and Bulk CMOS 6T SRAM cells' resilience to radiation effects. Both cells were simulated using TCAD tools, considering heavy-ion impacts in different locations of the transistor as well as using different impact angles. Two types of radiation effects have been considered: Single-Event Transients (SETs) and Single-Event Upsets (SEUs). The minimum critical collected charge (CC) to flip a cell is almost the same in both technologies. However, it is shown that a FDSOI SRAM cell needs a heavy-ion impact with a Linear Energy Transfer (LET) around 10 times greater than a Bulk-CMOS SRAM cell, to generate a similar CC and to flip a cell.

1. Introduction

Silicon on Insulator (SOI) devices are candidate for future applications in several domains. The buried oxide (BOX) and the ultra-thin silicon body provide devices with a good drain induced barrier lowering (DIBL), sub-threshold slope and low threshold voltage variability. In particular, the Fully Depleted SOI (FDSOI) [1] is a two-dimensional device compatible with the current Bulk-CMOS manufacturing processes.

The space environment is full of charged particles and cosmic rays that can cause unexpected effects on electronic circuits. The alpha particles and heavy ions can produce Single-Event Effects (SEE) on circuits. The SEE have several classes, but only two are considered in this work: Single-Event Transients (SETs) and Single-Event Upsets (SEUs) [2]. For these phenomena, the transient current $I_p(t)$ produced due to alpha particle or heavy ion impact on a reversed biased p-n junction is modeled by:

$$I_p(t) = I_0[\exp(-t/\tau_F) - \exp(-t/\tau_R)] \quad (1)$$

where I_0 is the current generated by the charges, τ_F is the collection time constant of the junction, and τ_R is the time constant for initially establishing the ion track [3,4]. Fig. 1 shows an example of transient current, where $\tau_F = 20$ ps, $\tau_R = 1$ ps, and $I_0 = 350$ μA. The total collected charge in this transient is 6.65fC.

SRAM cells are circuits, which store one bit until their bias is turned off. The number of transistors per memory cell depends on the technology node and desired reliability. The SRAM cell with 6 transistors (6T SRAM) is the most common circuit in industry, due to good trade-off between fabrication costs, die size and reliability. There are other types of SRAM cells with more reliability, like the 10T and 11T SRAM cell [5,6], but these cells use more transistors, increasing the chip area occupied by the memory.

In this work, 28 nm FDSOI and 32 nm Bulk NMOS devices are simulated to observe the effects of heavy ion impacts and to verify the most sensitive locations of these devices to SET [2]. With this information it is possible to model a 6T SRAM in Data Retention Mode, and to obtain the Critical Charge (the minimum charge to flip an SRAM cell) due to a heavy-ion impact on the cell's largest transistor.

The rest of the paper is organized as follows: Section 2 describes the devices created using Synopsys Sentaurus TCAD tools. Section 3 explains the simulation setup to obtain the critical impact location and the results of these simulations. Section 4 describes the design of each 6T SRAM cell and the Static Noise Margins (SNM) of each circuit. Section 5 shows the simulations and results of the 6T SRAMs reliability to heavy-ion impacts. Finally, Section 6 presents the conclusions of this work.

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http://dx.doi.org/10.1016/j.microrel.2016.07.133
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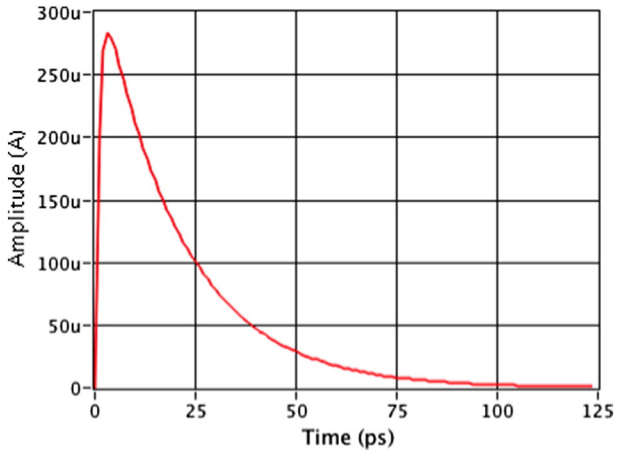

Fig. 1. Transient current example modeled using Eq. (1). The total collected charge is 6.65fC.

2. Tested device structures and characteristics

The first step in our study is creating the devices for comparing the SET effects. The use of the Sentaurus TCAD tools is necessary for our study because these tools simulate the phenomena occurring in the internal device structure to a heavy-ion impact and not only its effect [2]. As the driver transistors are the devices with the largest area in an SRAM cell [7,8], only the NMOS transistors have been created, as in a 6T SRAM the probability of heavy-ion impact on the NMOS transistors is the highest in the circuit. A comparison of resilience between these technologies to heavy ions was done in [2].

To perform these comparisons, a 32 nm Bulk NMOS device was created based on the 32 nm Bulk-CMOS PTM Low Power SPICE Model Card [9]. Fig. 2 shows this device. In this device the gate oxide thickness is $t_{ox} = 1.3$ nm, the total raised terminal height is $T_{RT} = 60$ nm, and junction depth is $x_j = 50$ nm. The gate length is $L = 32$ nm and the effective length is $L_{eff} = 30$ nm. The Drain/Source wells have a 4.36×10^{20} cm^{-3} n-type doping with a Gaussian profile; meanwhile the substrate has a 4.12×10^{18} cm^{-3} p-type constant doping. The poly-silicon metal-gate work function is $\Phi_{MS} = 4.25$ eV [2].

The 28 nm FDSOI node has some common electrical characteristics with the 32 nm Bulk-CMOS Low Power node [9]; Fig. 3 shows the modeled device. The device parameters have been chosen based on the process description [14] to match the Bulk-CMOS $I_D(V_G)$ characteristics; they are $L = 26.8$ nm, $L_{eff} = 21.4$ nm, $T_{Si} = 8.5$ nm, $T_{RT} = 18.5$ nm, $T_{BOX} = 20$ nm (Buried Oxide layer), $T_{BP} = 25$ nm (Backplane), $t_{EOT} = 1.83$ nm. The Drain/Source wells have a 4.4×10^{20} cm^{-3} n-type Gaussian doping profile; the Channel/Body of the device has a 1×10^{15} cm^{-3} p-type constant profile; the backplane layer (BP) has a 2×10^{18} cm^{-3} constant doping, the substrate has a p-type constant doping profile of 1×10^{14} cm^{-3}. In this case the metal-gate work function is $\Phi_{MS} = 4.52$ eV [2].

Table 1 summarizes the electrical parameters of both created devices. The bias (saturation) voltage is $V_{dd} = 1$ V. The voltage to test the linear region is $V_{dd} = 0.1$ V.

Fig. 4 shows a comparison between the I_d vs. V_g characteristic curves of the Sentaurus TCAD devices and the 32 nm Bulk NMOS SPICE Model in saturation ($V_{dd} = 1$ V).

3. Heavy ion impact simulation on tested devices

To simulate the heavy-ion impact on FDSOI NMOS transistors (a SET effect simulation), the devices were configured in off state, i.e. $V_{drain} = 1$ V, $V_{source} = V_{gate} = V_{substrate} = 0$ V. A heavy ion with Linear Energy Transfer (LET) of 100 MeV-cm^2/mg was chosen for all the simulations. The impacts were performed on the drain, source [2] and gate regions,

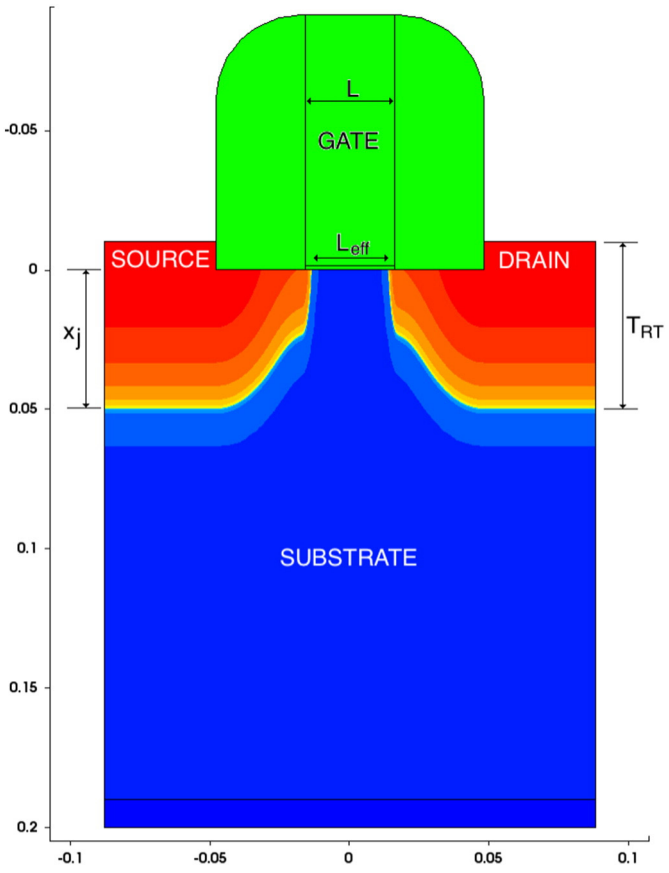

Fig. 2. 32 nm Bulk transistor structure.

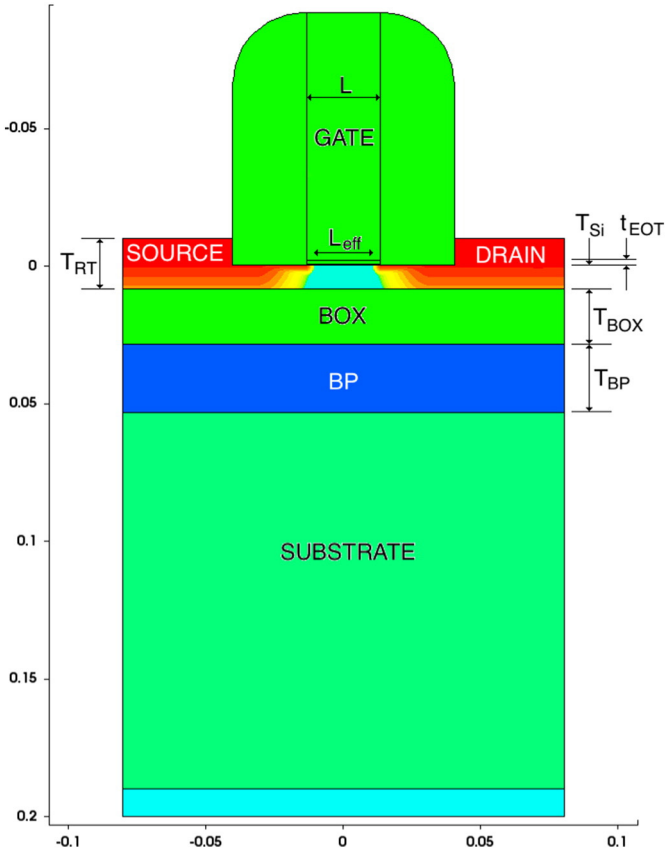

Fig. 3. 28 nm FDSOI transistor structure.

Please cite this article as: W.E. Calienes Bartra, et al., FDSOI and Bulk CMOS SRAM Cell Resilience to Radiation Effects, Microelectronics Reliability (2016), http://dx.doi.org/10.1016/j.microrel.2016.07.133