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Performance vs. reliability adaptive body bias scheme in 28 nm & 14 nm UTBB FDSOI nodes

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ABSTRACT

This paper shows the advantages of using body bias. Experiments are performed in 14 nm and 28 nm UTBB FDSOI transistors and ring oscillators (ROs). The impact of body bias on performance and reliability is highlighted. The body biasing offers significant advantages for adapting the tradeoff between reliability and performance in logic circuits without changing the design margins. With FDSOI technology, we have an additional degree of freedom of process variability compensation by using body bias voltage (Adaptive Body Bias, ABB) next to supply voltage compensation used before. We show that ABB compensation technique presents better results for a complete power optimization.

1. Introduction

For more than 50 years, CMOS technology scaling is still the fundamental driver of microprocessor industry. This law paces the device roadmap, as defined within the ITRS consortium [1]. That is why advanced CMOS such as Ultra-thin Body and BOX (UTBB) FDSOI (Fully Depleted Silicon On Insulator) technologies have been introduced at 28 nm and 14 nm nodes to provide both enhanced speed and reduce power consumption. These improvements were possible thanks to superior electrostatic behavior [2,3] due to fully depleted channels, as in FinFET device architecture.

We present here reliability results showing that FDSOI technology shows similar reliability than other nodes while offering the unique capability to enable body bias voltage modulation which acts as a second independent gate (Fig. 1). UTBB FDSOI technology allows a new adaptive compensation technique between performance and reliability based on a large dataset obtained both in 28 nm and 14 nm UTBB FDSOI devices and Ring Oscillators (ROs). We investigated degradation mechanisms as Negative Bias Temperature Instability (NBTI) and Hot-carrier Injections (HCI) involved in 28 nm and 14 nm UTBB FDSOI nodes, the potential benefit of using forward and reverse body bias on MOSFET and ROs are demonstrated. Finally, we present new process and aging compensation techniques.

2. Device and circuit reliability

The MOS transistors and Ring Oscillator circuits tested in this paper are with gate-length L_{nom} = 14 nm and 28 nm developed by STMicroelectronics company. This technology operates under double gate configuration with a body bias applied at a ground plane under bulk oxide (BOX) that enables to modulate the threshold voltage (V_{th}). Fig. 1 shows V_{th} evolution as a function of body bias (V_b) under forward (FBB) and reverse (RBB) configurations. The use of FBB mode allows the decrease of V_{th} whil RBB mode increases V_{th}. With the BOX thickness (25 nm), V_b can be higher than ±4 V (Fig. 1), being about 10× greater than in bulk devices technology without compromising the BOX integrity.

2.1. Negative bias temperature instability

PFet devices are stressed at 125 °C under AC NBTI conditions with a 50% duty cycle using various V_g and V_b stressing voltages. Threshold voltage degradation (ΔV_{th}) is measured in two kinds of PFet devices with L_{nom} = 14 nm and L_{nom} = 28 nm in Fig. 2, as a function of V_g stress variation. From their time dependences, V_g stress power-law and time exponent n are extracted. We find that these technology nodes follow same V_g stress power-law and have a close time exponent value giving n = 0.22 for 14 nm and n = 0.19 for 28 nm node.

NBTI V_g-stress dependence allows the extrapolation of V_{max} operating voltage as the nominal supply voltage for V_g = 0.945 V for 14 nm and 1.155 V for 28 nm PFet node. We observe that for a 10 year lifetime

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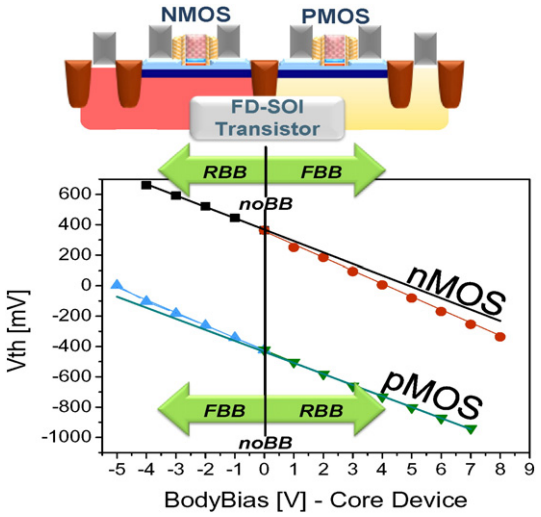

Fig. 1. V_{th} modulation by body bias V_b under forward mode FBB where V_{th} decreases and reverses mode RBB (V_{th} increases) for core N-P-Fets.

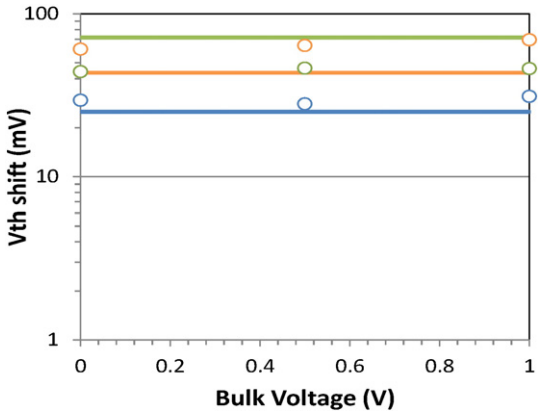

Fig. 3. NBTI shows no dependence with sensing body bias V_b for various supply voltages in 28 nm FDSOI PFets.

operation 14 nm and 28 nm nodes have the same NBTI damage ($\Delta V_{th} \approx 10$ mV) when they operate at V_{max} (full squares in Fig. 2).

To study the possible impact of sensing body bias (V_b) under NBTI, V_{th} degradation is plotted as a function of V_b in Fig. 3. We evidence that NBTI degradation is not influenced by V_b sens applied during stress.

14 nm and 28 nm PFet UTBB FDSOI nodes are compared in Fig. 4 to previous Si bulk CMOS nodes with $L_{nom} = 130$ nm to 28 nm. NBTI parameters such as V_g power exponent, time exponent and device lifetime are compared. We observe that UTBB FDSOI with high-K metal gate technology presents NBTI behavior inline with other nodes in spite of a different device architecture. Similar observations have been done recently on FinFET devices, showing the universality of NBTI degradation across various device architectures.

2.2. Hot carrier injection (HCI) features

For hot-carrier tests, two kinds of experiments are performed in UTBB FDSOI NFets with $L_{nom} = 14$ nm and 28 nm as it represents the worst HCI damage. Firstly, various values of V_g/V_d stress are used while keeping constant V_b during DC stressing. Secondly, a constant V_g/V_d stress value is used for different values of V_b in FBB mode. The saturation current (Id_{sat} or I_{on}) degradation is measured at V_{dd}, V_b along tests under forward mode in order to compare the channel length effect between 14 nm and 28 nm FDSOI nodes.

Fig. 5 shows that I_{on} degradation in NFets under HCI stress increases with the increase of $V_g = V_d$ stress and V_b stress increase. At the same time, we see that UTBB FDSOI 14 nm and 28 nm NFets have the same V_d stress power law ($=4.6$) and very close V_b stress power law dependences (≈ 2.4). By varying V_d, we have an increase in carrier density but a strong increase in carrier energy as well. V_b modulation results in carrier density increase and V_{dsat} increase that decrease the pinch-off region extent and carrier energy [4,5]. It is also worth noting that the degradation penalty under FBB operation can be also modulated by V_b sense effect [6] with proper V_{th} lowering that screens the HCI and NBTI damage. We can conclude that the use of V_b allows the improvement of the trade-off between I_{on} performance versus reliability in 14 nm and 28 nm UTBB FDSOI technologies. Compared to other CMOS nodes, no increase in HCI damage is found in Fig. 6 despite the channel-length reduction down to 14 nm FDSOI.

2.3. Ring oscillator (RO) circuit reliability

To understand the benefit of digital circuit operation under FBB mode, we performed long-term wafer level stress on 101 stages Low-V_{th} based ROs designed in 14 nm and 28 nm UTBB FDSOI nodes.

In Fig. 7, ROs in 28 nm FDSOI technology are stressed at V_{dd} stress = 1.8 V under varying AC conditions, including duty cycle and frequency

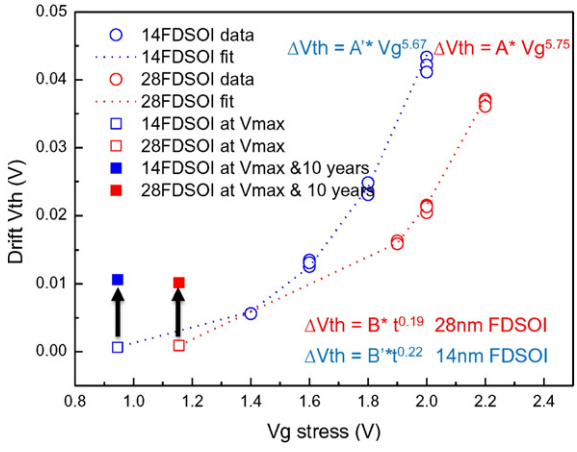

Fig. 2. ΔV_{th} vs. V_g stress and time power law in 14 nm and 28 nm PFet devices stressed under NBTI at 125 °C.

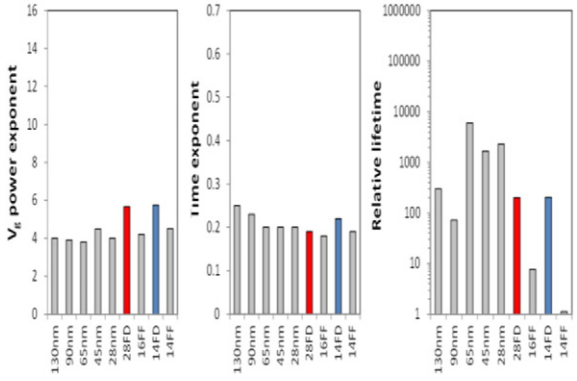

Fig. 4. FDSOI PFets with $L_{nom} = 28$ nm and 14 nm show no aggravated NBTI behavior compared to previous CMOS nodes. The red label indicates high-K metal gate appearance, while the blue label focuses on latest 14 nm FDSOI node. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

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