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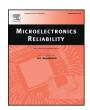
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On the prediction of radiation-induced SETs in flash-based FPGAs

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ABSTRACT

The present work proposes a methodology to predict radiation-induced Single Event Transient (SET) phenomena within the silicon structure of Flash-based FPGA devices. The method is based on a MonteCarlo analysis, which allows to calculate the effective duration and amplitude of the SET once generated by the radiation strike. The method allows to effectively characterize the sensitivity of a circuit against the transient effect phenomenon. Experimental results provide a comparison between different radiation tests data, performed with different Linear Energy Transfer (LET) and the respective sensitiveness of SETs.

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1. Introduction

The aggressive scaling trend in the nanometer technologies has significantly impacted the rates of Single Event Transients (SETs) faults within electronic circuits. When Flash-based FPGA devices are considered, the main concern is related to radiation-induced voltage glitches or SETs in the combinational logic. SETs may propagate through the circuit logic and be sampled by register or memory elements. If latched, they provoke single or multiple errors depending on the fan-out stems from the radiation-affected point. Errors may have critical consequences on the overall FPGA behaviour. In order to protect user memory and registers against these errors, several mitigation solutions have been proposed such as Triple Modular Redundancy (TMR) and Error Correction Code (ECC) [1]. Unfortunately these techniques were not able to protect circuits against SET, therefore different methods were proposed in the last decade in order to evaluate and model the SET phenomena. Recently, a SET-based fault injection approach for Bulk technology has been presented in [2]. This approach presents a strong novelty since it correlates the generation of the SET-pulse with respect to the radiation Heavy-ion strike; unfortunately this method is not applicable to Flashbased technology.

On the other hand, an accurate layout-based modelling of the SET phenomena is mandatory in order to correctly identify its intrusiveness within a circuit. In [3] an analytical method for the modelling and mitigation of multiple SETs has been proposed. However, this method is

mainly based on the probabilistic calculation of the transient pulse effect while it is not able to correlate the Linear Energy Transfer (LET) of the radiation particle strike with the effective generation of the SET phenomena. Thanks to the Heavy-ion experimental radiation test campaign performed in [4], we were able to evaluate the mitigation capabilities of place and route-based SET mitigation algorithms proposed in [5]. However, these methods applied to a realistic scenario are not effective. State-of-the-art mitigation approaches do not provide accurate information about the real source of the SET phenomena, therefore mitigation solutions may be over-estimated and inefficient with respect to the realistic type of pulse generated by a given radiation particle strike.

This work proposes an efficient methodology to predict the SET phenomena and to correlate its behaviour against the type of radiation energy, expressed in the form of LET (i.e., measured in MeV). The developed method has been validated by experimental analysis comparing the prediction achieved by the developed method with heavy-ion radiation test results with an uncertainty of 4.5% \pm 0.2%.

2. SET physical dynamic simulation models

The developed approach is based on two analytical models. The first one is the SET generation model which is used to generate the original SET pulse with respect to the LET value. The second approach is physical dynamic model. This model is used to dynamically describe the propagation behaviour considering the SET pulse is applied at the input of a gate.

2.1. SET generation

The incident particle has a scattering path during its penetration in the material, as shown in Fig. 1. If the particle has an energy higher

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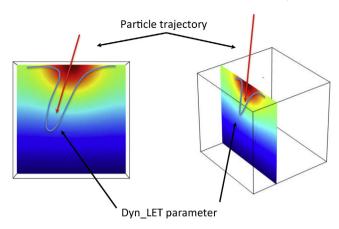


Fig. 1. An example of dynamic LET form on a generic empty layout in 2D and 3D.

than Δ , it can cross the material and create the voltage glitch inside the device that is called SET. Therefore, the dynamical energy of a particular particle incident on a material is defined as its energy loss per unit path length of penetration into the material itself, formula (1).

$$Dyn_{LET} = {}^{-dE} / _{ds}$$
 (1)

 Dyn_{LET} is defined as the particle incremental energy (dE) loss per incremental distance (ds) traversed in the material.

The SET generation model has been developed by a software module that correlates the values of the energy transferred to the silicon and the maximal depth where the energy is transmitted. The overall relation between the LET and the description of the SET pulse is represented by the formula (2):

$$\Delta V_{pulse}(GATE) = k_{gate} * (t_{pLH} - t_{pHL})$$

$$t_{pHL} = t_{SET} / D_{VRLFT}$$
(2)

In which t_{pHL} and t_{pLH} are the propagation behaviour relating to the gates. ΔV_{pulse} corresponds to the maximum Voltage pulse generated by a radiation particle. It is important to note that the maximum voltage pulse is not only dependent on the transmitted LET but also on the material which it deposits its energy. This effect has been defined as a coefficient of k_{gate} . The dynamic behaviour of the developed model is expressed by the ratio between the static time of the SET pulse (t_{SET}) divided by the dynamic LET shape and it is calculated by means of a modelled dissipation function created accordingly to each gate layout. Fig. 1 illustrates an example of dynamic LET calculation which is computed on the basis of the considered radiation particle trajectory, position of the radiation particle strike and layout topology of the cell. Thus, the SET shape analytically depends on the cell sensitive points and from the energy and position of the radiation particle.

2.2. SET propagation behaviour

In the previous section, the SET generation with respect to LET was studied. In this section, the propagation of the generated SET has been investigated. Considering the physical dynamic model, we described the behaviour of a 0-1-0 transition, where the transient pulse broadening of a node is computed as the difference between the propagation delays. The propagation delay is defined as t_{pLH} for an output transition from logical "0" to a logical "1", while t_{pHL} refers to a high to low output transition [6]. The propagation delay is measured between 50%

transition points of the input and output waveforms modelled by the following formula:

$$\Delta t_p = t_{plH} - t_{pHL}$$

$$if \left(t_{SET} > (k+3)t_{pHL} \right) \rightarrow t_{out} = t_{SET} + \Delta t_p$$

$$(2)$$

Where the coefficients of the propagation delays of t_{pHL} and t_{pLH} are computed by a linear interpolation of the experimental characterization we performed in [4]. It is known that each gate has different propagation behaviour related to the difference between the propagation delays of t_{pHL} and t_{pLH} which the transient pulse broadening and filtering at a node is dependent to these values.

In order to perform the characterization analysis we used two modules: a signal generator and a scope. The signal generator is an Agilent 81110A-M2 330 MHz. It has been used in order to apply pulses at different frequencies and with different voltages. The scope is a LeCroy WaveRunner 44Xi model equipped with high-impedance calibrated probes and able to measure voltage transients larger than 200 ps with a time resolution of about 90 ps. The probes have been connected to the chip under evaluation to measure voltage and width of the generated transient pulses generated and that propagated through inverter logic gates.

In order to characterize the SET behaviour, we developed an environment considering 5652 chains of inverters. This environment allows observing the influence of a glitch traveling from the injected point at the start of the chain toward Flip-Flops. Considering the number of inverters used in the environment, the source SET duration and the measured pulse duration at the end of the chain, t_{pHL} and t_{pLH} can be calculated for each SET pulse. The result of this analysis is reported in Table 1.

Please consider that the SET pulses have been selected in order to physically perform an electrical injection analysis, therefore SETs are not considered for the proposed study since they are not possible to be generated by electrical injection approaches on 130 nm technology. However, our model has been created considering SET having width up to 0.2 ns thanks to the interpolation with the propagation behaviour estimated by physical electrical injection.

In order to inject SET, we use a methodology based on internal electrical pulse injection for accurate characterization of the SET propagation within the logic and routing resources of Flash-based FPGA [7].

The proposed methodology is based on an internal pulse generator designed to create SET pulses, which allows a better control of a SET parameters comparing to external injection. The internal electrical pulse generator consists of a logic scheme composed of one *inverter* gate connected to an *and* gate, Fig. 2. The Signal "SG" is connected through the input pad to the signal generator while the signal "IN" is connected to the start of the chain. By inserting more than one single inverter, it is possible to generate wider pulses. Since the generator proper functioning strictly depends on the timing characteristics of its nodes, we had to accurately tune them for generating the expected pulse. We performed

Table 1 Propagation behaviour.

Input pulse [ns]	Output pulse [ns]	t _{pHL} [ns]	t_{pLH} [ns]
19.57	26.83	2.793	2.791
12.35	18.68	1.763	1.761
8.33	16.69	1.188	1.186
4.25	12.383	0.605	0.603
3.34	12.461	0.466	0.464
2.49	12.588	0.354	0.352
1.89	12.324	0.267	0.26575
1.35	12.251	0.214	0.216
0.84	12.132	0.192	0.198

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