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Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability

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ABSTRACT

In this paper, reliability issues of Stacked Gate (SG)-Gate Electrode Workfunction Engineered (GEWE)-Silicon Nanowire (SiNW) MOSFET is examined over a wide range of ambient temperatures (200–600 K) and results so obtained are simultaneously compared with conventional SiNW and GEWE-SiNW MOSFET using 3D-technology computer aided design quantum simulation. The results indicate that two temperature compensation points (TCP) are obtained: one for drain current (I_{ds}) and other for cut-off frequency (f_T) where device Figure Of Merits (FOMs) become independent of temperature, and it is found at 0.65 V in SG-GEWE-SiNW in comparison to other devices, hence will open opportunities for wide range of temperature applications. Furthermore, significant improvement in Analog/RF performance of SG-GWEW-SiNW is observed in terms of I_{on}/I_{off}, Subthreshold Swing (SS), device efficiency, f_T, noise conductance and noise figure as temperature reduces. It is also observed that at low temperature SG-GEWE-SiNW unveils highly stable linearity performance owing to reduced distortions. These results explain the improved reliability of SG-GEWE-SiNW at low temperatures over GEWE-SiNW MOSFET.

1. Introduction

CMOS devices are extensively used in the field of satellite communications, military, medical equipment, automobile, nuclear sectors, and wireless/mobile communications. For these applications and the demand of nanoscale transistor, it is important to investigate the device behavior at a wide range of temperatures [1]. Also, it has been demonstrated that the performance of MOS devices significantly improves when operating at low temperatures in terms of improved carrier mobilities, on-currents, gain, sub-threshold slope, cut-off frequency, short-channel effects and noise performance [2,3]. The unwanted flow of high leakage current through the junction and the presence of latch-up put a limit on the use of bulk MOS devices at high temperatures. Several technologies have been reported in the literature as an option for both low and high-temperature operations. Some of them are Silicon on Insulator (SOI) [4], Recessed Channel [5], III–V semiconductors [6], Nanowire transistors [7], etc. Among them, SiNW emerged as most favorable in electronic devices due to the fact that its concentration, dopant type can be changed during synthesis. Also, its mobility is higher than bulk silicon due to stronger 1D quantum confinement. The body thickness of the nanowire can readily be reduced to a few nm in size that is the major challenge to achieve using bulk silicon. Also, since hot carrier degradation is a major concern for short channel MOSFETs [8], several engineering schemes are reported in literature such as gate metal workfunction engineering [9], drain engineering and channel engineering to overcome this degradation. Moreover, the high-k gate dielectric is required for suppressing the leakage current with scaling of gate oxide. The high-k gate stack also improves Short Channel Effects (SCEs) and increases I_{on}/I_{off} ratio in sub-100 nm regime. Therefore, a novel device is proposed in which stacked gate architecture is implemented on Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET. In this work, for the first time performance and reliability issues of SG-GEWE-SiNW MOSFET are examined in terms of Analog, RF/Noise and Linearity FOMs at different temperatures (200–600 K) with an aim to analyze the temperature at which the device is more reliable for analog and RF applications. The results so obtained are simultaneously compared with GEWE-SiNW and SiNW MOSFET. Section 2 explains the 2D cross-sectional view of three different device structures including all the necessary boundary conditions. In Section 3, all the default simulation models are described along with the calibration of simulation models with experimental results. Section 4 contains the results obtained by device variation at 200–600 K and conclusions are drawn in Section 5.

2. Device structure and its description

Fig. 1(a) shows the simulated 3-D device structure of SG-GEWE-SiNW MOSFET and its 2-D cross-sectional view along with GEWE-SiNW and SiNW MOSFET are shown in Fig. 1(b–c). The detailed

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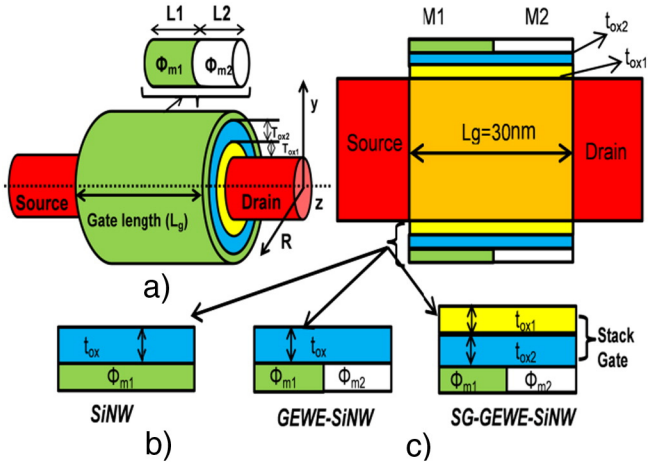

Fig. 1. (a) Simulated device structure of SG-GEWE-SiNW MOSFET, (b–c) 2-D schematic view of SiNW, GEWE-SiNW and SG-GEWE-SiNW MOSFET.

descriptions of all the three device structures are listed in Table 1. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator.

With GEWE (workfunction transition) scheme, there is a significant reduction in the SCEs, current driving capability improves due to step potential which is due to two dissimilar metal gates, reduced electric field at the drain end thus providing hot-carrier reliability [10]. Further, we have already shown that integration of GEWE scheme onto GAA-SiNW MOSFET improves device efficiency, enhanced on-current, reduces short channel effects [11,12]. Moreover, Table 2 lists all the boundary conditions associated with the device structure.

3. Simulation methodology

All simulations have been performed using the ATLAS device simulator [13]. The physical models used during simulations are shown in Table 3. Moreover, the quantum confinement in the sub-nm scaled device may not be negligible [14] because the inversion layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension. Thus, the quantization effect is also taken care of in the simulation. To incorporate all non-local effects, we have adopted the quantum mechanical models which are more accurate than drift-diffusion method. The Bohr Quantum Potential (BQP) Model [15] with alpha (α) = 0.5 and gamma (γ) = 1.2 was used to taking quantum mechanical effects into consideration. This model introduces a position dependent quantum potential, Q, which is added to the Potential Energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics [16] and is described below:

$$Q_{eff} = \frac{-\hbar^2}{2}\gamma\nabla\frac{\left[M^{-1}\nabla(n^{\alpha})\right]}{n^{\alpha}} \quad (1)$$

where M^{-1} is the inverse effective mass tensor, α and γ are two adjustable parameters, n is the electron (or hole) density and h is a Planck's constant. Additionally, numerical methods such as BICGST (bi-conjugate gradient stabilized) have been considered to obtain the solutions with improved convergence in 3D device structure [13]. Default simulator coefficients for all parameters have been employed. To fairly analyze the device performances, all the three devices are optimized to have the same threshold voltage, i.e. 0.4 V by changing channel doping. The calibration of model parameters used in simulation has been performed according to the experimental results [17] and closed proximity of simulated results with the experimental results as shown in Fig. 2 validates the choice of parameters invoked during simulation.

4. Results and discussion

4.1. Analog performance

In this sub-section, the analog performance of all three device structures is studied under different temperatures (200 K–600 K) with an aim to analyze the reliability issues in terms of analog FOMs such as on-current, device efficiency, switching ratio, Subthreshold swing (SS) and Threshold Voltage (V_{th}). Fig. 3(a) shows the transfer characteristics of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures. With the increase in temperature, the drain current rises but at a particular bias point, current starts decreasing with increase in temperature. This point is called Zero Crossing Point (ZCP) or Temperature Compensation Point (TCP). At this point, the effect of temperature is cancelled by two main controlling terms i.e. channel mobility (decreases I_D) and threshold voltage (increases I_D), since the temperature dependency of the drain current is influenced by V_{th} as given by $I_D \approx \mu_{eff}(T)\,[V_{gs} - V_{th}(T)]$. The TCP is desirable for wide temperature IC applications where the V—I characteristics show little or no variation with respect to temperature. With the increase in temperature, the on-current decreases due to degradation in mobility of carriers owing to more scattering of carriers. However, on-current of SG-GEWE-SiNW is comparatively high in comparison to GEWE-SiNW due to the incorporation of thin layer of HfO_2, which improves current driving capability of the device. The switching ratio is an important parameter for digital and analog applications and it is clearly evident from Fig. 3(b) that with an increase in temperature switching ratio degrades in an exponential manner for all three devices since phonon scattering is dominant at high temperature which degrades off-current. SG-GEWE-SiNW shows better switching performance in comparison to GEWE-SiNW due to lowering of tunneling carriers owing to gate stack engineering. Fig. 3(c) shows the device efficiency as a function of drain current for different temperatures. It is observed that device efficiency degrades in all three devices as temperature increases due to enhanced drain current in the linear region.

Fig. 4(a) indicates that the threshold voltage (V_{th}) degrades with an increase in temperature due to shift in Fermi level and band-gap energy. In general, MOSFET's I—V characteristics are proportional to the square of the overdrive voltage. Hence, a small change in V_{th} causes a significant

Table 1
Default design parameters used in the analysis.

Design parameters	SiNW	GEWE-SiNW	SG-GEWE-SiNW
Channel length (L_g)	30 nm	30 nm	30 nm
Substrate doping (N_A)	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Radius of nanowire (R)	5 nm	5 nm	5 nm
Source/drain doping (N_D^+)	5×10^{19} cm^{-3}	5×10^{19} cm^{-3}	5×10^{19} cm^{-3}
Effective oxide thickness (t_{ox})	$t_{ox} = 1.5$ nm	$t_{ox} = 1.5$ nm	$t_{ox} = 1.5$ nm $t_{ox1} = 1.2$ nm (SiO_2) $t_{ox2} = 1.85$ nm (HfO_2)
Dielectric constant	$k = 3.9$	$k = 3.9$	$k_1 = 3.9$, $k_2 = 24$
Gate metal work function	$\Phi_m = 4.8$ eV	$\Phi_{m1} = 4.8$ eV [Gold] $\Phi_{m2} = 4.4$ eV [Titanium]	$\Phi_{m1} = 4.8$ eV [Gold] $\Phi_{m2} = 4.4$ eV [Titanium]

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