Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Laser Voltage Probing (LVP) – Its value and the race against scaling

Ulrike Ganesh

Qualcomm Technologies, Inc., 5775 Morehouse Drive, San Diego, California, USA

ARTICLE INFO

Article history:
Received 27 June 2016
Accepted 7 July 2016
Available online xxxx

Keywords:
Laser Voltage Probing
LVP
VLI
Electro-optical Probing
Laser Timing Probe
LTP
Frequency mapping
Modulation mapping
Effects
Interference
Signal generation
Benefits
Challenges
ITRS
Scaling
FinFET
GAA
3D

ABSTRACT

After providing a brief introduction to Laser Voltage Probing (LVP), along with useful information and further reading suggestions, this paper provides a deep dive into current benefits and challenges of LVP applied to 16/14 nm FinFET technology and discusses the issues that arise from scaling of technology nodes according to the International Technology Roadmap for Semiconductors.

1. Introduction to LVP

Laser Voltage Probing (LVP) is an all-optical, contactless and destruction-free fault isolation technique that employs photons to optically measure the electrical device activity, such as signal levels of a switching transistor and corresponding timing information, through the thinned silicon substrate. It has developed into a well-established method that is used for device characterization and electrical fault isolation as part of product debug in failure analysis.

Harley K. Heinrich's dissertation, "A noninvasive optical probe for detecting electrical signals in silicon integrated circuits" [1], written in 1987, can be seen as the foundation of LVP. In the 1990s, the technique was integrated in a system and hence became commercially available to failure analysis labs.

Since its first introduction, setups have been (re-)implemented with various detection schemes – Mode Locked Laser [2], Continuous Wave Laser [3], Polarization Difference Probing [2], phase- [2] and amplitude-sensitive [1] detection schemes etc. –, improved measurement methods – Voltage Sweeping with spectrum analyzer [3], Modulation Mapping or Laser Voltage Imaging [3], lock-in amplifier for Sign Mapping [4], high speed digitizer and logic analysis [5] – and derived applications, such as Laser Logic State Imaging [6]. A more detailed overview of the history and various detection schemes can be found in [7]. Depending on the tool supplier and/or the setup used, different technical terms have been established in the community – besides "Laser Voltage Probing" and its derivative "Laser Voltage Imaging", this technique is also known as "Laser Timing Probe/Measurement" and its derivative "Frequency Mapping", as well as "Electro-optical Probing" (Fig. 1). Essentially, these terms are interchangeably.

The general principle is based on the interaction of the laser beam with the device under test. A laser scanning microscope (LSM) can be used as the basic platform for the system. Current setups employ a near infrared (NIR) laser (usually 1319/1340 nm or 1064 nm), which is focused through the (thinned and polished) silicon backside of the device, which is partially transparent for NIR laser radiation.[1] For this

E-mail address: ulrikek@qti.qualcomm.com.

[1] See [8] for details about how thinning of the silicon bulk helps to improve the transmittance, but note that full thickness measurements are possible depending on the doping level and thickness of the bulk.

http://dx.doi.org/10.1016/j.microrel.2016.07.054
0026-2714/

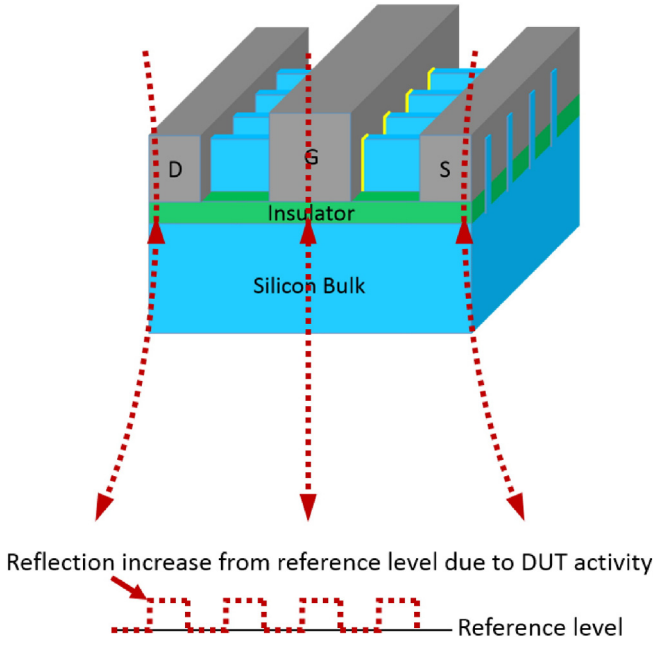

Fig. 1. FinFET model with contacts to Drain (D), Source (S) and Gate (G). Not to scale. The laser beam (dashed lines) is incident through the backside of the device (through the silicon bulk). When the device is off, the reflection is at some reference level (used for LSM image), when the device switches, the reflection is modulated due to the device activity (waveform) – here a simplified schematic shows the amplitude modulations of the laser radiation.

purpose, multiple air gap lenses with different magnification factors and a solid immersion lens (SIL), which makes contact with the thinned silicon, are used. The portion of the laser radiation that has not been absorbed by the bulk is incident on the active areas of the device and reflected off the interfaces in the depth of focus. The reflected laser radiation is detected by a photo detector. The relatively strong static part of the reflected radiation is used to generate an image of the device (LSM image). The reflected radiation also consists of a modulated part (amplitude and/or phase modulations; much lower in intensity, in the parts-per-million range), if the device is active, since the optical parameters of the device are altered by the device activity. This modulated part of the reflection is the actual LVP signal.

The reflected radiation intensity is a result of multi-beam interference. A detailed explanation of the signal generation process including multi-beam interference/interference effects can be found in [9]. The intensity of the reflected radiation at each interface is dependent on the optical material properties (index of refraction and absorption coefficient), which in turn depend on other parameters. Some of those are setup-dependent (e.g. laser wavelength), some are independent of the device activity (strength and orientation of the built-in electric field, measurement temperature, charge carrier density of bulk, diffusions etc.) and others are modulated by the device activity (*change* in temperature, electric field, free carrier concentration etc.). In addition, the device activity changes parameters that are affecting the interference effects directly, such as the variation of the space charge region thickness. An attempt to model and simulate the reflectance from an active device as well as a more detailed description of the signal generation process and its dependency on device and setup parameters can be found in [7,9].

2. Significant benefits of LVP

One of the benefits of LVP begins with the accessibility of the nodes of interest: it allows access across the whole device without the need for expansive sample preparation. For example, no probe hole/pad generation is necessary and most times simple thinning and polishing of the backside is sufficient. This makes LVP a fast, non-destructive and contactless data collection technique, which does not cause any capacitive load on the node.

The wide spectrum of derived setups and methods enable many different use cases for LVP, but the main application is the signal extraction as part of the electrical fault isolation flow. Scan chain debug is such an example: if a signal line (chain of inverters) is broken at a specific point, which is yet to be determined, a Laser Voltage Image (LVI or Frequency Map) can determine which inverters in the chain are active and from where on the signal is interrupted. Other applications are timing measurements and logic pattern extraction.

LVP is a versatile technique that has been proven to work on many different devices (bipolar transistors [1], MOSFETs, diodes and MOS varactors [9]), technology nodes and types of technologies (e.g. 350 nm bulk and FinFETs with elevated S/D diffusions out of the bulk [10], as well as SOI [11], also see issues with SOI probing in the same publication) and is even usable for wafer-level probing, when used with a wafer stage (see offers for wafer stages from different vendors on their respective websites).

Generally, it is possible to extract signals from an active device, as long as the device activity causes changes in the reflectance.

Also note that steady state measurements – as in Photon Emission Microscopy's Logic State Imaging – are not possible, since the signal is generated by the *changes* of parameters with device activity. However, an intelligent measurement technique can enable the extraction of quasi-static signals (see [6] for information on Laser Logic State Imaging) and the setup described in [5] enables the collection of large amounts of data in order to analyze the logic state of a node.

In comparison to Photon Emission Microscopy, another well-established electrical fault isolation technique, the signal-to-voltage correlation is not exponentially dependent on the device voltage, but instead it is mostly linear (however not reliably, see [9] for some voltage sweeps) and signals can currently be measured down to about 50 mV, which is greatly dependent on the setup, the device etc.

Higher sensitivity towards low level signals can be achieved by using a lock-in amplifier setup, as it was described in [4].

3. Challenges with LVP

Even though there are a lot of challenges with the measurements, the preparation and set up of the device are a major concern and require a lot of time. The first requirement for LVP measurements is that the chip backside region is accessible to the laser beam, while at the same time, the device has to be connected electrically. For stand-alone flip chip devices this is trivial, since the backside of the die in the package is only covered by the package, which can be removed/opened in order to access the device backside. For packaged devices (maybe even with a memory on top) that are integrated in a test platform (e.g. mother board connected to a daughter card with a socket etc.) this can be a non-trivial task, since most times, design for test and debug is not a requirement at earlier design stages and hence the chip that is supposed to be measured is not exposed, but maybe hidden under a board or obstructed by components. It is of tremendous help if the socket with the exposed chip backside is the highest point of the setup and free of obstructing components, since lenses, especially the SIL, need to be placed close (on top) of the backside of the device. Designing a new board in order to enable LVP measurements is time-consuming and expensive and can be avoided by planning for characterization and debug.

In case, the device needs to be thinned and polished, a couple of different techniques are available (see e.g. [12]). Usual sample thicknesses for NIR laser setups are around 100 µm, but some SILs may require sample thicknesses as thin as 50 µm. For such thin devices, warpage is a major concern: the thickness is not uniform across the entire die and hence the requirements for the SIL may not be met (worst case: no

Please cite this article as: U. Ganesh, Laser Voltage Probing (LVP) – Its value and the race against scaling, Microelectronics Reliability (2016), http://dx.doi.org/10.1016/j.microrel.2016.07.054