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Static logic state analysis by TLS on powered logic circuits: Three case studies for suspected stuck-at failure modes

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ABSTRACT

Thermal Laser Stimulation (TLS) for static logic state analysis is applied to failure analysis. Three case studies of analyses of the digital logic in an automotive Application Specific Integrated Circuit (ASIC) are discussed. By analyzing the logic states of the circuit we were able to identify the mechanism and localize the site of irregular behavior non-destructively, both for a stuck-at fault and two weak interconnects. The approach measures the power supply current while applying TLS to the device back side. This allows an extremely high analysis coverage, because every transistor is connected to the power supply, making this method a universal tool for every digital circuit failure analysis (FA) workflow, because the gained understanding of the fault allows to replace multiple steps of alternative FA techniques by only a single technique, reducing time and cost for successful FA.

1. Introduction

Suppliers to the automotive industry are confronted with strict zero-failure requirements. To cope with these targets, successful failure analysis of each individual failing part is essential to success as well as demanding expectations concerning analysis speed. As a consequence, failures must be identified and localized by use of non-destructive methods first. Ideally, the physical root cause should be understood from these methods, which is often a difficult and time consuming task. Nevertheless, the more information gained through these techniques, the better the chance to make the right decision for subsequent analysis steps, which have a potential risk to irreversibly change or even destroy the sample (e.g. Focused Ion Beam (FIB) pads). This preserves the failing part, which may be the only one of its kind, in its original state, hence making destruction-free analysis techniques a key asset.

For situations where signals cannot be put into a repetitive situation (i.e. operational loop), many techniques (i.e. E-beam Probing [1], Laser Voltage Probing [2], Photon Emission Microscopy) become unavailable. Laser stimulation can be set up such that the device is operated statically and information about the logic state is derived. This has first been published in a security and reverse-engineering context [3], and has been suggested as a means for conducting failure analysis [4]. The present work proves the applicability of TLS on powered devices to failure analysis and points out major benefits.

2. Thermal Laser Stimulation (TLS)

TLS is applied by observing an electrical device response while scanning a laser with a wavelength larger than 1100 nm over the device surface [5,6]. This is commonly known as Optical Beam Induced Resistance Change (OBIRCH) or Seebeck Effect Imaging (SEI), depending on the physical connection between laser stimulation and electrical circuit response [5]. In these cases the devices are unbiased or only partly biased (e.g. by a single pin or micro-probing pad). This reduces the available area for inspection to those parts of the circuit electrically connected to the measured terminal. An improved analysis coverage can be achieved when measuring the power supply current instead: Each part within a digital integrated circuit (IC) is connected and therefore can be measured. This approach is often applied when locating IDDQ (quiescent digital supply current) failures: the fault location will react very sensitive to TLS.

Previous works [4,3] have shown that even more information can be derived, because *every* transistor, even intact ones, within the circuit reacts to the stimulation by the laser. However, it requires appropriate acquisition methods and interpretation of the results to make use of this information. The TLS response from intact transistors is analyzed in this work according to the procedure described earlier [3], for the first time in an FA context. Although the analysis of intact transistors within an FA context seems ill-placed, the presented three case studies show that valuable information can be gained by this technique.

3. Interpretation of TLS images for logic state analysis

The supply current is monitored, either by an AC coupling amplifier or by a lock-in amplifier. Bright spots in the resulting scan image

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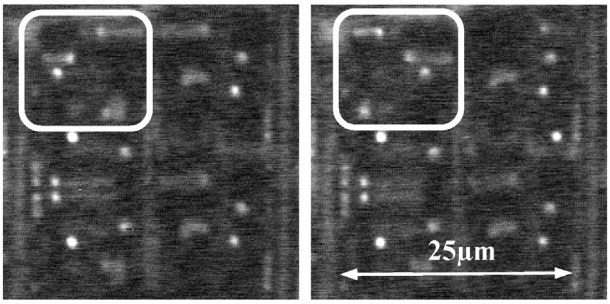

Fig. 1. Device response to TLS acquired on power supply of digital part in two different states. The rectangle corresponds to the register which changes state between two images.

correspond to locations with a higher current consumption during the stimulation by laser. The sensitivity of a transistor depends on its logic state [4]. Thus, when changing the information stored within the gates, the observed TLS response changes as well.

Two images are acquired from two different logic states. The logic states are chosen such that the gate of interest is changed while as much of the remaining circuitry as possible is kept unchanged. As a result, the acquired images only differ within the gates of interest. Subtracting the two images from each other shows the difference in logic states within the device. This technique has been described as a tool for reverse engineering IC [3] and suggested for FA [4]. Once the device behavior and image properties are known, signals can also be compared between nearby transistors. The subtraction of two images in different states and the comparison of nearby transistor requires quantitatively comparable signals. The presented TLS signals originate from the transistor structures. By pointing the laser to the silicon back side of the IC ("back side analysis"), the signal path between stimulation and measurement is alike for all transistors. As a consequence, the signal fingerprints are quantitatively comparable.

The two states can be chosen by various ways. In this work, we achieved good results by identifying one state where the gate of interest behaves incorrectly. This could be a certain vector within a digital test pattern. The corresponding second state is then selected as the last correct vector state prior to the incorrect state. The resulting difference image can already contain indications for the irregular location.

4. Devices and setup

The devices from this case study are manufactured in a 350 nm CMOS process designed specifically for automotive applications. For the TLS logic state analysis, the devices were set up within a Laser Scan Microscope (LSM) equipped with a 50× Near Infrared (NIR) optimized lens (NA = 0.76) and a high luminosity laser diode with a wavelength of 1300 nm. The devices are brought into the various logic states

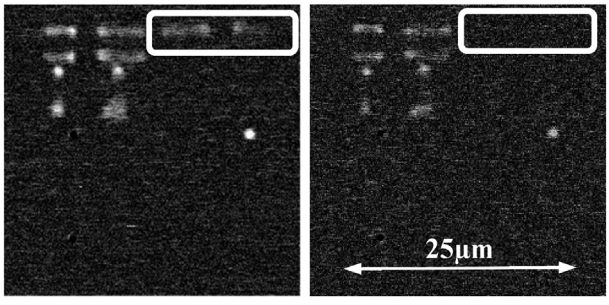

Fig. 2. Detailed view of the register with the stuck-at fault in the failing device (right) and comparison with a reference device (left). The register stores the two possible states (0 and 1) but the output driver (rectangle) does not track the state correctly in the failing device.

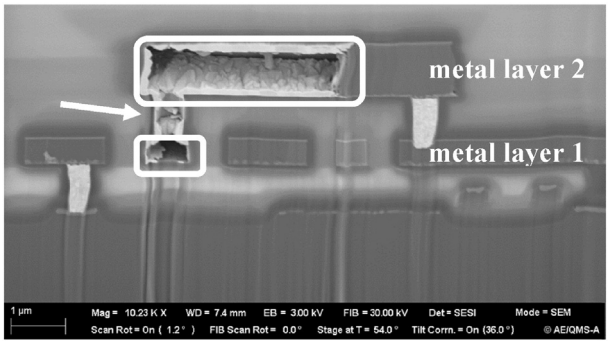

Fig. 3. In the Scanning Electron Microscopy (SEM) image of the FIB cross-section a defective via (arrow) and missing wires on metal layers 1 and 2 (rectangles) were identified as reason for the observed behavior of case #1.

by an automated test equipment while the power supply of the digital part was monitored with an AC amplifier or a lock-in amplifier.

5. Case study #1: stuck-at fault localization

A digital test pattern analysis suggested a stuck-at fault in one of the circuit's registers. A test pattern was designed to alter the contents of the suspected register while leaving the remaining logic states untouched. The register location was identified with this approach on a reference device. Fig. 1 shows the two images acquired with a state of '0' and '1' stored within the register. The corresponding difference image is shown in Fig. 2 (left image). The register is connected to a tri-state driver, which also shows up in the images (rectangle in Fig. 2).

The same analysis was carried out on the conspicuous device. The difference image shows an identical fingerprint for the register but misses the output driver, see Fig. 2. As a consequence, the path to the register is intact and the anomaly is located at the output driver. In a Focused

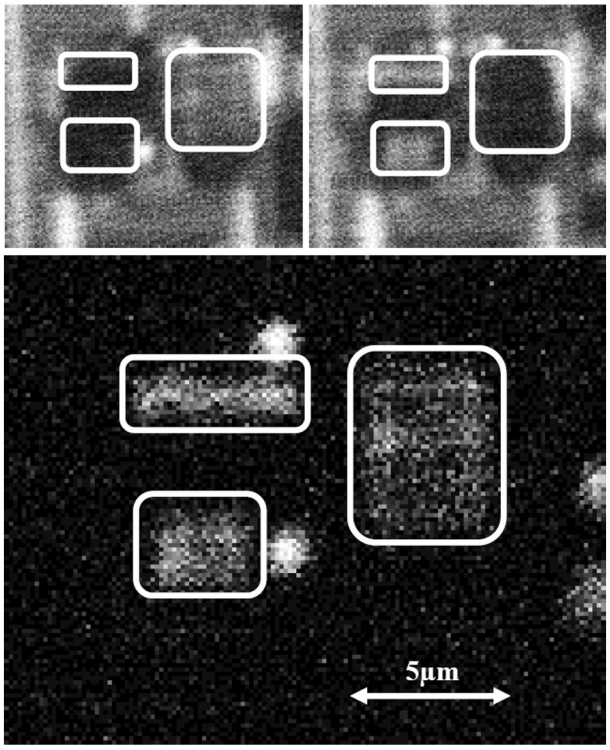

Fig. 4. TLS response images (top) and resulting differential image (bottom) of the suspected gate (same Field of View, FOV). The gate's output transistors (rectangles) change state, excluding a hard stuck-at fault.

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