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200 V Fast Recovery Epitaxial Diode with superior ESD capability

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ABSTRACT

In this paper the Electrostatic Discharge (ESD) capability of 200 V Fast Recovery Epitaxial Diodes (FREDs) is analysed by means of suitable experiments, TCAD simulations and theoretical analyses. Different doping profiles are investigated in order to improve the ESD robustness of a standard device and an optimized doping profile is proposed. The newly fabricated devices show a remarkably high ESD capability without any significative loss in forward voltage drop and a reduction of the breakdown voltage that does not affect device rating.

1. Introduction

The use of power semiconductor devices in highly demanding environments such as the automotive industry is showing an increased demand for qualified devices which can withstand strong electrical overstresses during their handling and operating lifespan. Actually, the ESD robustness for power diodes in the field of automotive is one of the most important parameters for the device selection during power circuit design. While avalanche operation of power diodes is a very well assessed field, the ESD ruggedness of vertical devices has not received the same deal of attention. A power diode is usually designed to meet static, such as Forward Voltage (VF) and Breakdown Voltage (BV), and dynamic performances like the reverse recovery behaviour [1]. On the other hand, as no critical oxide layers are present in a power diode structure, it is common sense to avoid extended testing of these devices to ESD events, or to demand for proper grounding of operators during handling operations.

In this work we have tested for ESD ruggedness a FRED Diode designed to sustain 200 V and we have analyzed the distribution of the failures as a function of voltage. The inspection of the physical signatures of the failure mode suggests the onset of the typical current filamentation caused by the presence of Negative Differential Resistance (NDR) branches in the reverse bias IV curve [2,3]. As it has been demonstrated [4–6], this can lead to current filamentation and eventual failure of the device and they are caused by the backside injection of carriers due to second breakdown of the N−/N++ transition between Epi-layer and Cathode [7]. The adoption of a buffer layer to increase the avalanche robustness is widely adopted for bipolar power devices such as IGBTs [4,8], as well as power diodes [7] where the double injection effect is only related to the impact ionization effect. Since latter mechanism can be mitigated by the insertion of a specially engineered buffer layer at the N−/N++ transition, new devices with different buffer layers have been fabricated and the experimental validation of the proposed design is carried out.

2. ESD test and failure signatures

The ESD robustness of the devices under test was experimentally evaluated by the circuit in Fig. 1, in Human Body Mode (HBM-ESD) [9]. C and R are the most relevant lumped elements of the ESD test and they schematize the typical human impedance. $C_{para}1$, $C_{para}2$ and

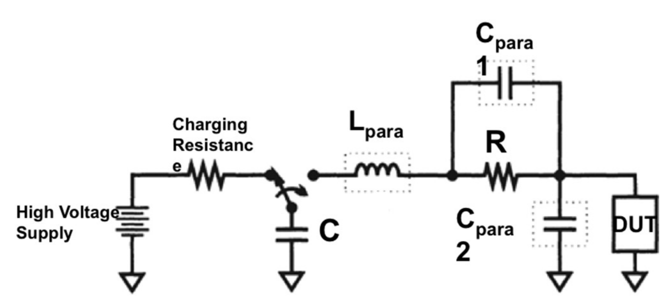

Fig. 1. A sketch of the ESD tester in HBM configuration for the experimental characterization.

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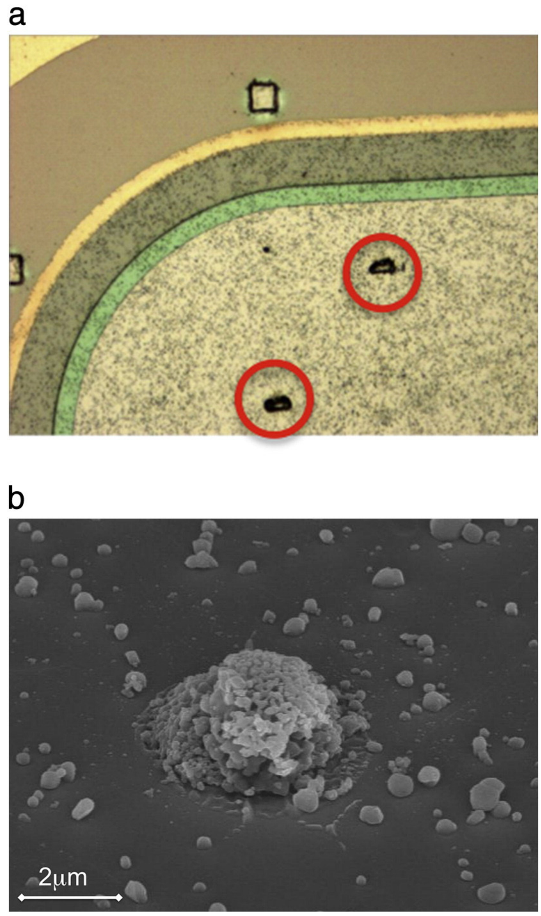

Fig. 2. (A) A typical failure during the ESD test for the 200 V rated diodes (B) and a detail of the burned area.

L_{para} are parasitic elements, not relevant for the analysis presented in this work. The HBM-ESD test is divided in two steps. In the first step the C capacitance is charged at a high voltage by means of a high voltage power supply. In the second step the C capacitance is connected to the right hand side of the circuit. The human body equivalent resistance is emulated by the resistance $R = 1.5$ k Ohms and C = 100 pF.

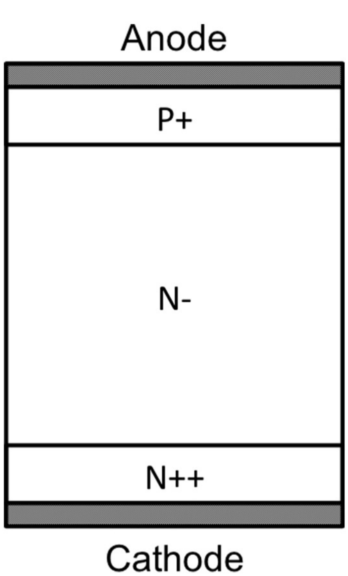

Fig. 3. A sketch of the power diode structure.

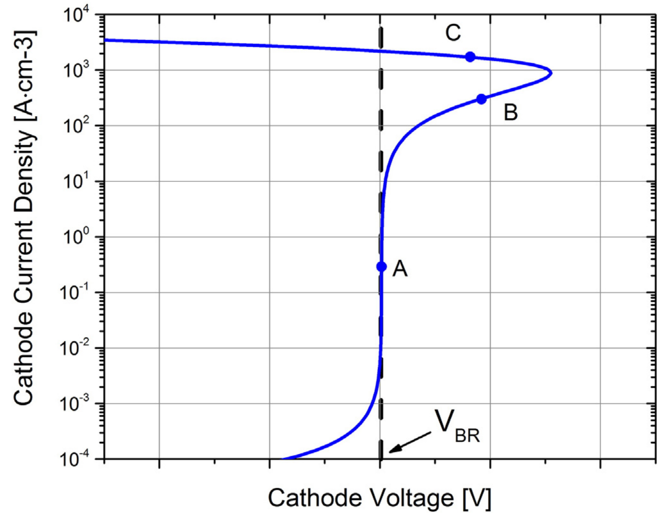

Fig. 4. IV curve of the power diode.

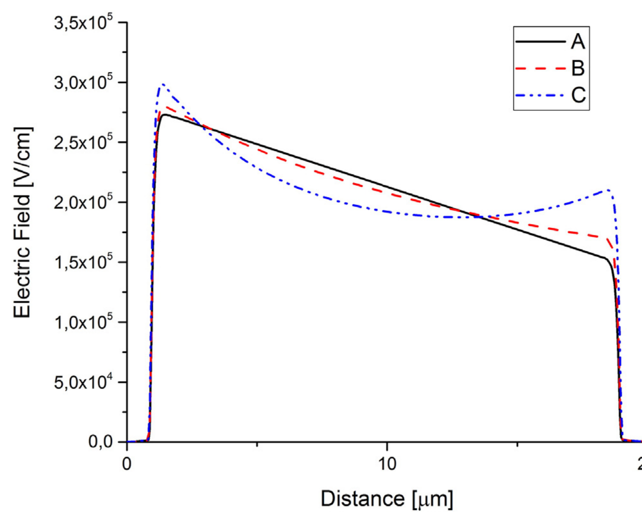

Fig. 5. Electric field distribution in the points A, B and C of Fig. 4.

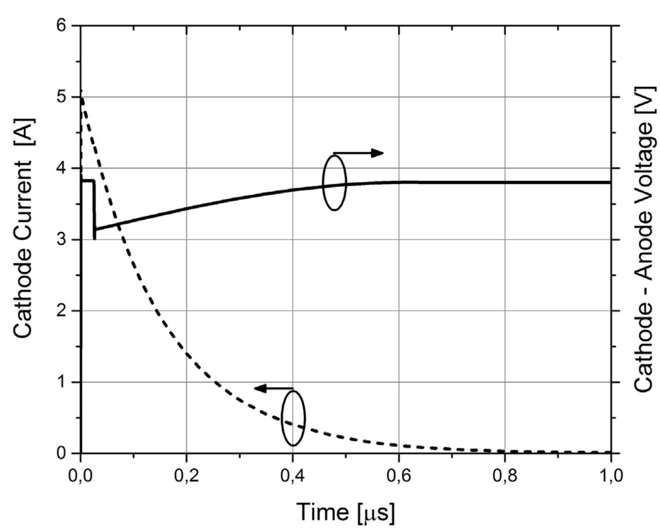

Fig. 6. ESD waveform for the large area structure with $V_C = 8000$ V.

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