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Topologies for inverter like operation of power cycling tests

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1. Introduction

In standard power cycling tests the devices under test are always in on-state during the heating period. The load current is switched by external switches to control on-period for heating and off-period for cooling down the devices.

The conduction losses' temperature coefficient depends on device and working point. Thereby beginning degradation of the die attach and bond wire interconnect either partly compensates or amplifies the temperature swing ΔT_j, when the load current is kept constant throughout the power cycling test. As a consequence, the degradation mechanisms are either de- or accelerating themselves depending on the working point and the characteristic of the device. Tests on low-voltage Si-MOSFETs published in [1] showed a five times lower power cycling capability, when they were tested in MOSFET mode compared to body diode-mode at the same initial temperature swing ΔT_j and a control strategy of constant load current and on-period. The current per bond-foot was three times higher in MOSFET-mode, which according to CIPS2008 model would only estimate a factor of two for lifetime. In contrast to conduction losses, switching losses as they occur in the application of power devices always rise with temperature, regardless of device and working point.

More dedicated test benches, in which devices under test switch on and off themselves in an inverter-like topology had been used in [2,3]. There the DC-voltage was set to high-voltage. Switching against high voltage has several advantages. The measurement delay t_{md} for measurement of the maximal junction temperature T_{jmax} after turning off the load current can be reduced [3]. The capability of switching load current (RBSOA) of the devices under test is proven throughout the lifetime. External switches are not needed. However, high DC-voltage brings some disadvantages. Despite safety issues, which need to be addressed, measurement accuracy is limited [4]. This led to the idea for the test bench with inverter-like topology as described in Section 2.1. Another extended approach is to switch the devices under test in a similar setup at high frequency. Thus, switching losses significantly contribute to the losses. This allows lowering the current and getting closer to application conditions. Section 2.2 covers this new approach.

2. Test bench topologies

2.1. Inverter-like topology with low DC-voltage

In the test bench according to Fig. 1, six half-bridges are connected in a topology similar to a three-phase inverter. The current paths are similar to an inverter circuit, meaning load current to flow from the DC(+)-terminal to the AC terminal of one half-bridge and to enter the second half-bridge at the AC terminal and exit at the DC(−)-terminal. Differing from inverters, each DC connection consists of a long cable which inhibits a stray inductance L_σ. Thus, when a device under test (DUT) turns off a voltage pulse is induced across it. The DC bus is powered by a 20 V source. Two operation modes are implemented to cycle the power losses and related temperatures.

An “inverter like” operation, where each H-bridge is crosswise switched at a frequency of up to several Hz, before the next H-bridge is operated in the same way. Operation at high frequency would need severe changes in topology (large main inductance L_M) and measurement system as described in Section 2.2. Switching one H-bridge means power cycle on-period. Keeping all switches off in one H-bridge means power cycle off-period. In other words the sequence for conducting the load current is alternating between (1_1, 1_4) and (1_2, 1_3), within H-bridge 1.
Then H-bridge 2 is operating in (2_1, 2_4) and (2_2, 2_3) paths. Finally the same applies to H-bridge 3, i.e. (3_1, 3_4) and (3_2, 3_3).
The switching operation within an H-bridge happens with a duty cycle of 50%. Power cycling, i.e. operation of H-bridge 1, 2 and 3 happens with a ratio of on-period to off-period of 1:2.

The other mode (“standard-like”) is closer to the operation in standard power cycling tests. There two IGBTs of each H-bridge are operated after another in the first half-cycle, before changing to the other two IGBTs of each H-bridge in the next half-cycle to complete one power cycle. The sequence for conducting the load current is (1_1, 1_4), (2_1,

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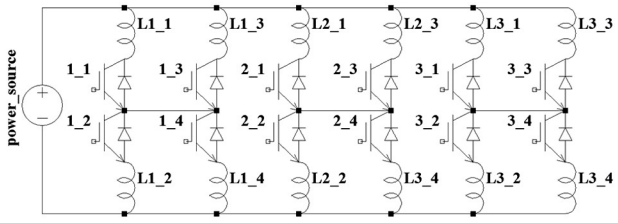

Fig. 1. Inverter-like topology for up to six half bridge-modules. For example, DUT 1_1 and 1_4 in the first H-bridge conduct load current, while DUT 2_1 in the second H-bridge is on for T_{jmin}-measurement and DUT 3_2 in the third is on for T_{jmax}-measurement, the others are turned off.

2_4), (3_1, 3_4) in the first half-cycle and then (1_2, 1_3), (2_2, 2_3), (3_2, 3_3) in the second half-cycle. Thus if the on-period is set equal for all DUTs, off-period is five-fold the on-period.

For measuring the junction temperature T_{vj} using the $V_{CE}(T)$-method a sense current is fed in one out of four IGBTs before and after operating its H-bridge. Therefore it takes four half-cycles before T_{jmin} and T_{jmax} are measured once for each.

For every DUT the pulse pattern consists of the following steps.

1) While the H-bridge before is being operated, a DUT in the present H-bridge turns on for T_{jmin}-measurement, the three other IGBTs in the same H-bridge are kept off.
2) After that, another DUT turns on in the same H-Bridge. The two H-bridges overlap for a selectable time of for example a few 10 µs.
3) The H-bridge conducting before turns off. The present H-bridge is operated with load current.
4) A DUT in the next H-bridge is turned on for T_{jmin}-measurement.
5) After that another DUT turns-on for overlapping.
6) The DUT and the other IGBTs of the present H-bridge turn off.
7) The DUT turns on for T_{jmax}-measurement and off again.

The voltage peak during turn-off is solely caused by the fall of current within the stray inductance. An overlap of high voltage and load current is achieved as for inductive load turn-off in an inverter. Representative switching losses occur by this kind of turn-off. Fig. 2 shows an example, where a current slope $di_c/dt = -125$ A/µs provokes a voltage peak $V_{CE,peak} = 200$ V at the IGBT, with $L_{\sigma,total} = 1.6$ µH.

The voltage peak is limited by the gate driver with active di/dt control, e.g. active clamping. The amplitude may be adjusted by selecting the clamping voltage and the size of stray inductance.

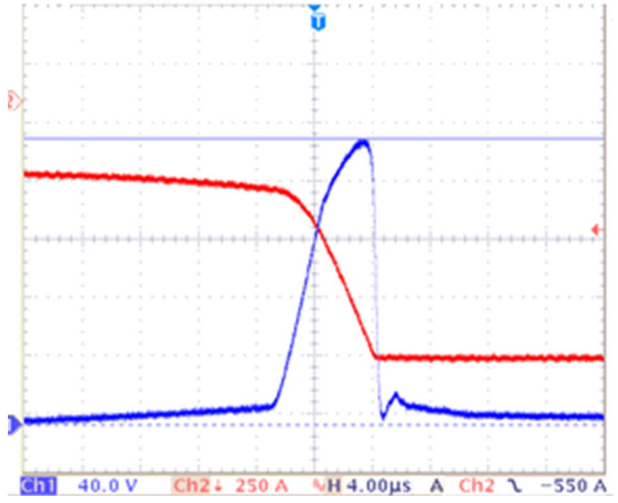

Fig. 2. Switching-off event at low DC-voltage, red: I_C from 750 A, 250 A/div; blue: V_{CE} limited to 200 V, 40 V/div; time 4 µs/div. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

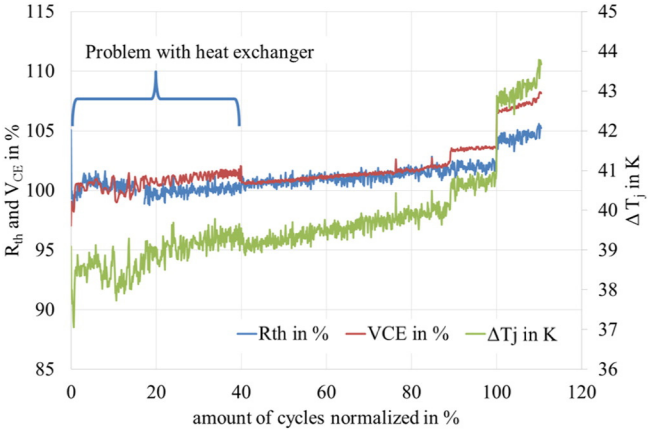

Fig. 3. Plot of V_{CE} and R_{th} and ΔT_j (measured at t_{MD}) of a test on FF900R12IP4D (Infineon Technologies AG) and $t_{on} = 60$ ms, $\Delta T_j = 39$ K ($t_{MD} = 1$ ms, $\Delta T_{j,error} = 4$ K), $I_{load} = 1000$ A, $T_{jmin} = 68$ °C.

Fig. 3 shows a plot of an end-of-life (EoL) test. $V_{CE}(I_{load}, T_{jmax})$ and R_{th} are plotted. Test conditions are: "standard-like" mode, $t_{on} = 60$ ms, $\Delta T_j = 39$ K (measured after measurement delay $t_{MD} = 1$ ms, $\Delta T_{j,error} = 4$ K), $I_{load} = 1000$ A, $T_{jmin} = 68$ °C. After more than 15 million cycles the EoL criterion 105% of initial V_{CE} was reached. The derived cycles to failure fulfill the expectation. For this test mode "standard-like" no deviation from standard power cycling tests was observed.

2.2. Test bench for high-frequency operation

A test method which allows free adjustment of switching to conduction losses ratio would help to investigate differences of power cycling modes. Additionally it would allow decreasing the average load current. This is especially interesting for low-voltage MOSFETs.

2.2.1. Concept of test bench

A test bench topology is proposed and being built where external switches alternate the load current in between two legs. One leg is depicted in Fig. 4. Again the circuit is powered from a low voltage source (15 V). A main inductance L_M is connected in series to it.

In each leg two devices under test are paralleled and switch alternately at a selectable high-frequency. A stray inductance L_σ causes the voltage peak at turn-off and thus induces switching-losses. A third device under test is connected in series, which stays on. If the ratio of switching to conduction losses is selected to be equal within DUTs 1_1 and 1_2, DUT1_3 should have the same temperature swing ΔT_j as the two alternating devices. A sense current source is connected to each

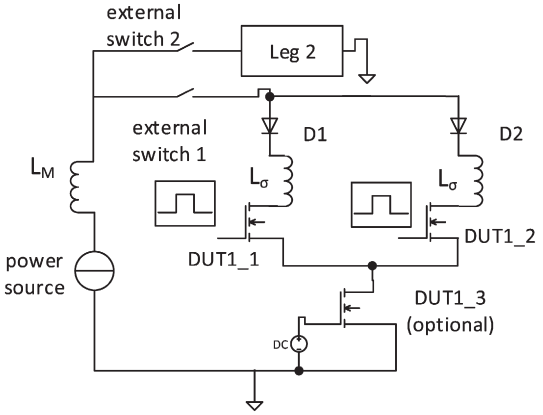

Fig. 4. One leg of test bench which enables heating by switching losses.

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