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End of life and acceleration modelling for power diodes under high temperature reverse bias stress

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ABSTRACT

This work is motivated by the growing importance of lifetime modelling in power electronics. Strongly accelerated High Temperature Reverse Bias (HTRB) testing of power diodes at different stress conditions is performed until alterations and fatigue mechanisms become evident. Two categories of effects can be separated: Drifting breakdown voltage and hard failures with complete loss of blocking capability. Nevertheless the overall stress duration needed to provoke destructive failures is very high with test durations >2500 h even at almost 230 °C and 100% rated voltage. For both mechanisms the temperature and voltage acceleration is evaluated. Especially temperature acceleration is significant in the regime of testing between 200 °C and 230 °C and an activation energy E_a in the regime >1 eV can be deduced which is higher compared to values commonly reported in the literature. Failure analysis shows that both package and also chip related effects could contribute to the observed hard failures in HTRB stress under extreme conditions.

1. Motivation

Acceleration models are needed to assess whether reliability stress tests are suitable to cover real life mission profiles. The need to include mission profile oriented qualification in the validation of products has become more pronounced during latest years which manifests itself among others by the introduction of the robustness validation concept [1] and also by the latest update of the qualification guideline AEC-Q101 [2] that includes a new appendix on "Guidance on Relationship of Robustness Validation to AEC-Q101". On the other hand proof for acceleration models is not always given and should be supported by more experimental data and understanding of distinct fatigue and failure modes. In this study we focus on High Temperature Reverse Bias (HTRB) stress aiming at strong acceleration by both voltage and temperature to investigate which intrinsic failure mechanisms can be provoked and how the acceleration can be modelled.

2. Experimental methods

2.1. Test structures

HTRB is a stress test commonly employed for power semiconductors, because high voltage stress is a typical load condition in power electronics. For the purpose of this study specific samples are built that can be tested even under harsh conditions exceeding by far the specified operation conditions of commercially available products. Fig. 1a shows a typical test structure containing 3 parallel silicon power diodes which are mounted in a modified Infineon Easy package, where an Al_2O_3 substrate represents the baseplate of the test module. The diodes' device area is small (merely 2.2×3.7 mm²) in order to limit leakage current losses and avoid thermal runaway of the thermal stack. Chip technology is based on the vertical concept of a 1200V silicon-PIN diode with p doped anode on the top side. The lateral junction termination is realized by means of a combination of field rings and field plates passivated by polyimide coating. The carrier profile of the diodes in conduction mode is optimized for fast switching by applying a combination of weekly doped emitter layer and moderate lifetime reduction of charge carriers. This diode design allows for a low level of leakage current I_R of typically 0.2 mA/cm² at specified operation temperature of 150 °C. The low level of I_R is a necessary prerequisite to enable HTRB testing at extreme temperatures without thermal runaway.

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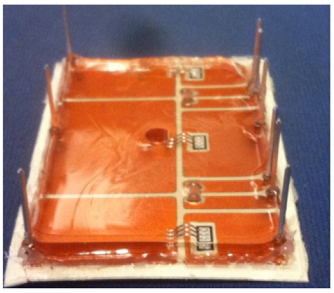


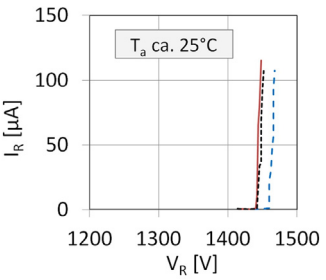


Fig. 1. a (left): Test structure without housing. Fig. 1b (right): Typical blocking characteristic at 0 h and T~25 °C for 3 diodes of one test structure.

To enable high temperature stress testing above 200 °C the die bond is realized by a sintering process and the encapsulating housing is made of a plastic material with especially high thermal stability to avoid loss of its mechanical stability during testing. Silicone gel is dispensed on top of the dies and the Cu metallization of the substrate. Since the blocking characteristic is used for PASS/FAIL evaluation during the stress test, the characteristic dependence of leakage current I_R on reverse voltage V_R is recorded for each diode at room temperature at the beginning of the test (example: see Fig. 1b) and at each interim readout.

2.2. HTRB test bench and test process

The test bench enables stressing of 2 × 6 test structures as described in Section 2.1. Each test structure is mounted on a block that enables both heating and cooling in order to control the heatsink temperature T_h. Each block has 3 thermocouples measuring T_h directly under the dies (Fig. 2a). During stress test the hottest temperature is automatically chosen for the control algorithm of 1 block.

Voltage is applied in parallel to all 3 diodes of a test structure but the leakage current is monitored individually and in case of failure the respective diode is separated from the array by a switch.

With increasing temperature the reverse currents I_R of the diodes increase exponentially and thereby the corresponding power loss, resulting again in a rapid temperature increase. So a big risk for thermal runaway exists. Hence a sophisticated algorithm that takes into account the dynamic of case temperature dT_c/dt, the virtual junction temperature T_{vj} and the dependence $I_R = f(T_c)$ is applied to mitigate the risk of thermal runaway. For this the individual characteristics $I_R = f(T_C)$ of each diode is recorded before test start and integrated into the control software in terms of parameters of an exponential function.

The temperature control for the heating/cooling blocks is performed sequentially with a control cycle of 15 s. With the information of the real time temperature trend dT_c/dt of the heating/cooling blocks and the individual temperature characteristics $I_R = f(T_c)$ the control software is able to predict the junction temperature of any diode at the next control cycle. So, if the predicted temperature of the hottest diode reached a critical limit at the next control cycle the temperature setting would be adjusted in advance.

At suitable readout intervals the devices are cooled down to room temperature with applied bias and the blocking characteristic is recorded to be sensitive to drifting breakdown voltages V_{BR}.

Table 1
DoE for voltage and temperature dependence.

	T = 200 °C	T = 230 °C
V = 1000 V	Not tested	18 diodes
V = 1200 V	18 diodes	18 diodes

2.3. DoE of stress parameters

Temperature and voltage are the dominating stress agents at HTRB. Typical qualification tests are running at V_R = 80…90% of the rated device voltage and T = 125…175 °C (depending on device rating) [2,3]. For the purpose of this study it is planned to raise temperature up to 230 °C and voltage up to 100% of the rated voltage at a nominal rating of 1200 V. The extreme case for which both parameters are kept simultaneously at these upper limits is studied. Furthermore either one parameter is kept at the mentioned upper limit whereas the respective other parameter is reduced to study it's influence. The experiment is aiming at the following DoE shown in Table 1 to allow for an assessment of both temperature and voltage acceleration. In the real experiment average temperature T_j of 197.5 °C and 226.5 °C have been achieved.

3. HTRB fatigue modes under extreme stress conditions

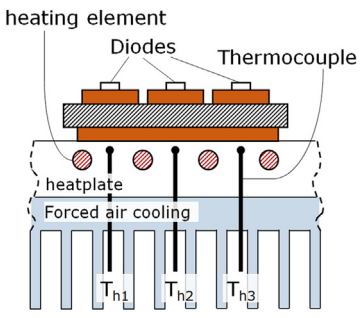
Two effects are observed that indicate alterations or aging of the devices by the implied stress:

i) V_{BR} is significantly drifting to lower values.

ii) hard failures with complete loss of blocking capability occur in a later phase when the drifts stabilize.

It is known that V_{BR} drifts strongly depend on the concept and the design of the termination structure, therefore for the purpose of this study a specific configuration of test design and passivation materials is chosen that exhibits clearly measurable drifts.

V_{BR} is recorded at room temperature at regular readout intervals after accumulated stress duration t_d passed. The ratio $V_{BR}(t_d)$ against the starting value $V_{BR}(t = 0)$ is calculated and displayed in Fig. 3 (226.5 °C/1200 V), Fig. 4 (226.5 °C/1000 V) and Fig. 5 (197.5 °C/1200 V) as a function of test duration t_d for the test conditions given in parenthesis. Both effects i) and ii) are visualized with $V_{BR} = 0$ indicating a complete breakdown of the blocking capability. We don't observe a clear correlation between maximum reached V_{BR} drift and the occurrence of hard failures, giving a first indication that both effects are caused by different mechanisms.



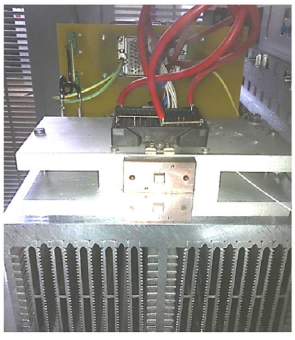


Fig. 2. a (left): Schematic cross section of test structure on heating/cooling block: Measurement of T_h directly underneath diodes. Fig. 2b (right): real test setup.

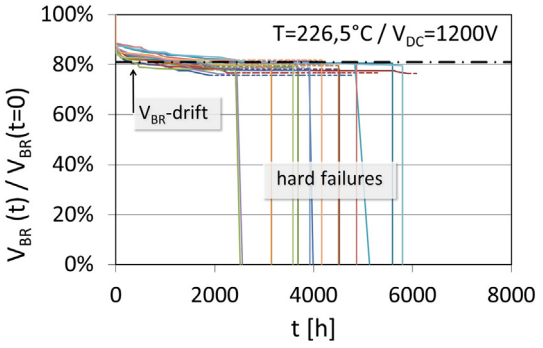


Fig. 3. V_{BR} drift effects observed at readout intervals and hard failures ($V_{BR} = 0$) at 226.5 °C/1200 V. The chain line at 81% indicates the drift criterion used in the statistical evaluation (same criterion as in Figs. 4 and 5).

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