Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Comparison of thermal runaway limits under different test conditions based on a 4.5 kV IGBT

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ARTICLE INFO

Article history:
Received 24 June 2016
Accepted 6 July 2016
Available online xxxx

Keywords:
Thermal runaway
IGBT
Thermal stability
Junction temperature

ABSTRACT

This investigation focuses on determining the temperature-dependent leakage current limits which compromise the blocking safe operating area for silicon IGBT technologies. A discussion of a proper characterization method for selecting the maximum rated junction temperature for devices operating at high temperatures is given by comparing the different testing methods: Static performance (including and excluding self-heating effects), Short Circuit Safe Operating area and High-Temperature Reverse Bias. Additionally, a thermal model is used to predict the junction temperature at which thermal runaway takes place. In this paper guidelines are proposed based on the correlation among short circuit withstand capability and off-state leakage current for guarantying reliable operation and ensuring that they are thermally stable under parameter variations. This study is helpful to facilitate application engineers for defining the correct stability criteria and/or margins in respect of thermal runaway.

1. Introduction

High-Voltage IGBTs are nowadays being pushed to operate closer and closer to their SOA (Safe Operation Area) limits at ever increasing temperatures [1,2]. With this new challenge, devices have to demonstrate their switching capability at the maximum ratings and specified junction temperature by proving their temperature-wise stable performances [3,4].

The definition of a maximum junction temperature in power semiconductor devices is a crucial topic for device designers as well as application engineers because it limits the stable operating range of such devices. For this reason, large margins are adopted to ensure the device reliability by derating the voltage and current of the device. Thermal runaway is one of the most common failure mechanisms in silicon semiconductor devices, especially at high temperatures in the off state [5]. As a rule of thumb, the leakage current for traditional-silicon devices increases by a factor of 2 when the temperature increases by 11 °C [6]. Thermal runaway is mostly related to technological issues, therefore it is worth mentioning the three leakage current main components: (a) the bulk of the IGBT chip (i.e., amplification behavior of the PNP transistor gain), (b) the chip termination design (i.e., p^+-type guard rings or variation of lateral doping), and (c) the passivation layers [7].

The main part of this study is to provide a guideline to select the rating of the maximum allowed junction temperature of semiconductor devices during standard operation $T_{vj}(op)$. In order to draw this conclusion, the devices must guarantee reliable operation and ensure that they are thermally stable even if they are exposed to parameter variations. To conclude that devices can be rated for a given temperature many factors should be considered, such as: thermal coupling from neighboring components, airflow, package materials and design, ambient temperature, good current/voltage sharing in paralleled/series devices, stable blocking behavior and low leakage current. Presently, the characterization method for defining the maximum rated junction temperature is to increase the temperature of the entire setup to the targeted operating temperature. Nevertheless, this method may give erroneous results because static stability criterions might be violated which are not relevant to the real-world applications.

Without losing generality, this study is based on 4.5 kV/150 A Soft-Punch-Through (SPT+) IGBTs by looking at thermal runaway failures. Two static stability methods and dynamic short-circuit tests are compared to find a cross-correlation under different tests conditions: a guideline has been proposed for defining the maximum junction temperature, based on the correlation between short circuit withstanding capability and off-state leakage current. Finally, a High Temperature

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http://dx.doi.org/10.1016/j.microrel.2016.07.025
0026-2714/

Reverse Bias (HTRB) test is also carried out in order to show the long-term reliability stability. This investigation is helpful to facilitate application engineers for defining the correct stability criteria and/or margins in respect of thermal runaway.

2. Static performance up to thermal runaway

2.1. Device under test

Experiments have been carried out on 4.5 kV/35 A SPT+ IGBTs which were mounted on test substrates similar to the one shown in Fig. 1. The test substrates consist of 4 IGBTs in parallel with two anti-parallel diodes. However, this study has been carried out on a single IGBT, thus the bond wires between the chips were removed.

2.2. Thermal stability testing methods

The IGBT leakage current was measured under blocking state at several operating temperatures by directly mounting the test-substrates on a temperature-controlled heating plate. In order to avoid the air gap between the substrate and the heating plate, pressure was applied.

Two test methods have been applied with the aim of illustrating the correlation among them, namely: (i) *IV*-sweep thermal stability test, and (ii) Quasi-static thermal stability test. For the *IV*-sweep test, the leakage current is measured when the blocking voltage is swept from 0 V up to 4.5 kV. The chosen voltage step from 0 V up to 2 kV is 100 V and then a finer voltage step of 50 V is selected. The pulse length at every point is 1.5 s and thus the chip self-heating effects are clear. On the other hand, the quasi-static test measures the leakage current by applying a single voltage pulse whose length can be programmed by the user. The voltage pulse has been selected to be 200 ms when the target junction temperature is below 140 °C and reduced to 20 ms above 140 °C, ensuring that the self-heating of the IGBT chip is negligible. Note that when the pulse length is too short, the leakage current will not have enough time to stabilize. Fig. 2 shows the IGBT leakage current values for the *IV*-sweep test and quasi-static test, for temperatures ranging from 100 °C up to 160 °C and from 75 °C up to 175 °C, respectively. Note that the test-substrates are mounted directly to the heating plate, thus, the initial junction temperature can be assumed to be similar to the heating plate's one. Both test methods are well-known; however, the correlation between them is usually not covered, especially when predicting the thermal runaway limits.

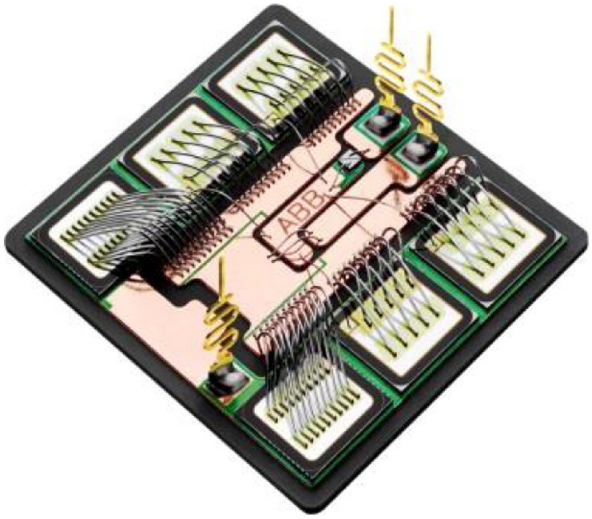

Fig. 1. 4.5 kV/150 A IGBT test substrate.

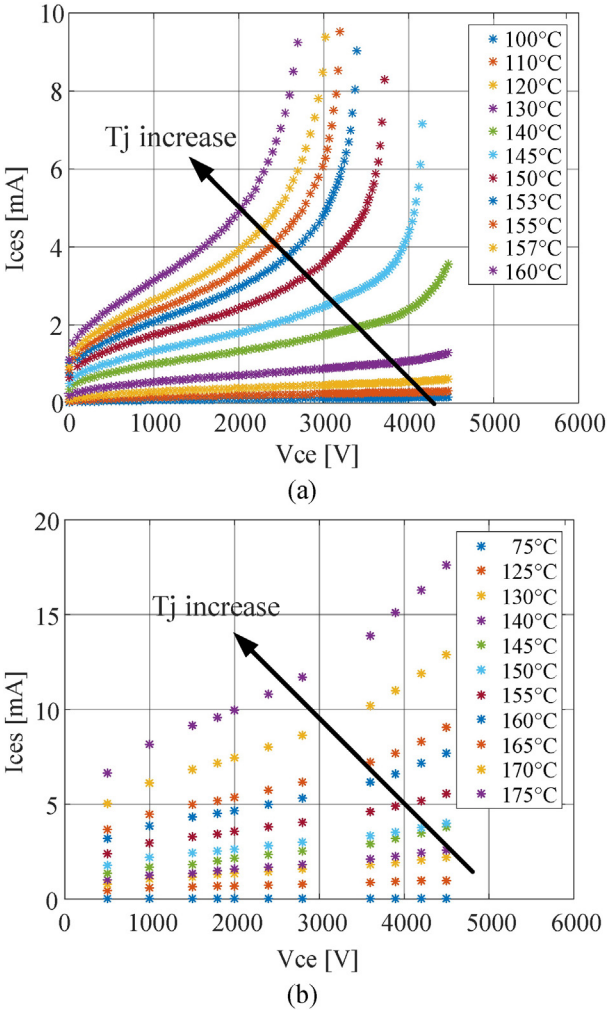

Fig. 2. 4.5 kV IGBT off-state leakage current dependence with temperature: (a) *IV*-sweep test (b) quasi-static test.

A significant conclusion can be obtained from Fig. 2. A correlation between off-state leakage current and junction temperature for a given blocking voltage can be made by applying the following formula [6]:

$$I_{CES}(T_1) = I_{CES}(T_0) \times 2^{\frac{T_1 - T_0}{\Delta T}} \quad (1)$$

where I_{CES} is the leakage current, T is the junction temperature of the chip and ΔT is the thermal coefficient obtained by fitting the curves in Fig. 2.

Thanks to this correlation, the leakage current can be estimated as a function of the junction temperature and included in the thermal models. Additionally, the differences between the two methods can be better understood. The data obtained from the *IV*-sweep method is R_{th}-dependent while the quasi-static method will give similar results independently of the cooling system.

2.3. Blocking stability criteria

Thermal runaway occurs when the heat generated is greater than the heat dissipated. To ensure thermal stability, it is essential that the relationship in Eq. (2) is not violated [8]:

$$dP_{gen}/dT_j \leq dP_{dis}/dT_j \quad (2)$$

The generated power P_{gen} is the one coming from the leakage current under the blocking state. The dissipated power P_{dis} depends on

Please cite this article as: P.D. Reigosa, et al., Comparison of thermal runaway limits under different test conditions based on a 4.5kV IGBT, Microelectronics Reliability (2016), http://dx.doi.org/10.1016/j.microrel.2016.07.025