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Design of two-stage nonrecursive rotated comb decimation filters with droop compensation and multiplierless architecture ☆

G. Jovanovic Dolecek[a,*], M. Laddomada[b]

[a]Department of Electronics, Institute INAOE, Puebla, Mexico
[b]Electrical Engineering Department of Texas A&M University-Texarkana, USA

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Abstract

This paper proposes a class of decimation filters with reduced passband signal distortion and improved spurious signal rejection across the folding bands. These filters are well-suited to decimation of oversampled digital signals processed by wideband digital receivers and $\Sigma\Delta$ AD converters. The total decimation factor is split between two stages of decimation and zero rotation in a nonrecursive form is applied at the lower rate in order to reduce the computational complexity of the proposed filters. We also address a framework to implement multiplierless filters and to compensate for the passband droop introduced by this class of filters. For increased flexibility, we generalize the transfer function by allowing different orders between the two stages of decimation.

The paper presents many examples to clearly describe the design procedure. Comparisons are also given with the goal of contrasting the magnitude responses of the proposed filters with the ones of three other techniques recently proposed in the literature, as well as with classical comb filters.

1. Introduction

Multistage decimation filters are important signal processing blocks in digital receivers [1–7] where they are usually employed in digital down-converters [8,9], as well as to decimate signals

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*Corresponding author.
E-mail addresses: gordana@inaoep.mx (G. Jovanovic Dolecek), mladdomada@tamut.edu (M. Laddomada).

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oversampled by $\Sigma\Delta$ Analog-to-Digital (AD) converters [10]. The first filtering stages in the decimation chain should be computationally efficient so as to limit power consumption given that these filters operate at high sample rate. Practically speaking, it is desirable to have multiplierless decimation filters accomplishing only additions and subtractions: this is the main reason for the use of comb filters [11] in multistage decimation architectures. Despite the computational efficiency, comb filters present magnitude response with poor attenuation around the folding bands, as well as a considerable passband distortion that deteriorates the processed signals.

The engineering applications we have in mind are related to $\Sigma\Delta$ AD converters as well as digital down-converter (DDC) devices. $\Sigma\Delta$ AD converters [10] are noise-shaping and oversampling AD converters that shape the quantization noise power spectral density in such a way that it results mainly located outside the frequency range of the useful signal. Noise shaping is accomplished through a feedback loop, while oversampling is employed to reduce the level of the quantization noise power density [10]. Decimation is used after the $\Sigma\Delta$ AD converter in order to select the useful signal while reducing its sample rate and filtering the quantization noise. The other application concerns DDCs, digital signal processing devices employed in wireless receivers to convert a digitized real signal centered around an intermediate frequency to a baseband complex signal centered around the zero frequency. These devices accomplish downconversion and decimation to a lower sampling rate.

In these applications, we wish to process a baseband real input signal $x(t)$ with analog bandwidth $[-B_x, +B_x]$. This analog signal is sampled by an AD converter with oversampling factor ρ. The notation employed in this work hinges upon the architecture in Fig. 1. The sample data rate at the input of the decimation block (output of the AD converter) is $f_o = 2\rho B_x$ where $\rho \geq 1$. With this setup, the maximum digital frequency in the input signal is $f_c = B_x/f_o = 1/2\rho$, thus mapping the analog frequency B_x to f_c upon sampling.

The oversampled signal is then decimated by M through an anti-aliasing decimation filter followed by a decimator by M. The digital bandwidth of the sampled signal is $[-f_c, f_c]$, as pictorially depicted in Fig. 1, while the frequency intervals

$$\left[\frac{n}{M} - f_c; \frac{n}{M} + f_c\right], \quad n \in \left\{1, \ldots, \left\lfloor \frac{M}{2} \right\rfloor\right\} \tag{1}$$

are called folding bands since any spurious signal falling within these bands will be folded down to baseband upon sampling. Therefore, in a multistage decimation architecture it is important to carefully design the frequency response of the anti-aliasing filter around these folding bands

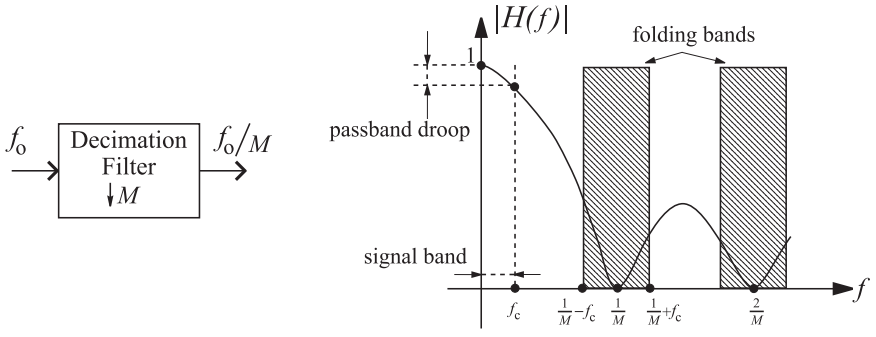

Fig. 1. Decimation stage along with a pictorial representation of the frequency response of the decimation filter $H(z)$ and the key frequency intervals to carefully consider in the design.

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