Applied Thermal Engineering 120 (2017) 347–357

Contents lists available at ScienceDirect

Applied Thermal Engineering

journal homepage: www.elsevier.com/locate/apthermeng

Research Paper

Simplified approach for steady thermal analysis of chips with variable power based on spatial autocorrelation

C. Pei *, G.C. Fu, Y.H. Zhao, B. Wan, Y. Cheng

School of Reliability and Systems Engineering, Beihang University, Beijing 100191, China

HIGHLIGHTS

- Approach for steady thermal analysis of chip with variable power is proposed.
- The determination of material properties and other factors can be tolerated.
- The highest temperature error in the case study is not more than 2%.

ARTICLE INFO

Article history:
Received 20 December 2016
Accepted 4 April 2017
Available online 5 April 2017

Keywords:
Steady thermal analysis
Spatial autocorrelation
Undetermined coefficient method
Power devices

ABSTRACT

Due to their growing power and shrinking size, thermal management and analysis have become one of the most critical concerns for power devices. Though finite element (FE) method is commonly employed in thermal analysis now, the uncertainty of material properties and the redundancy of repeat modeling still nag analyzers. In this paper, a simplified approach for steady thermal analysis of chips with variable power is proposed. Based on spatial autocorrelation and undetermined method, the steady temperature distribution could be directly determined with power distribution and example temperature measurement result, without identifying environment factors or material properties. The theory of the simplified approach is introduced at first in this paper. The characteristics of the simplified approach are discussed afterwards. Eventually, a case study is given to illustrate the procedure, of which the analytical result coincides with the actual measurement well.

© 2017 Elsevier Ltd. All rights reserved.

1. Introduction

As to the continual miniaturization and increasing power dissipation, thermal management has become a critical factor in the design process of microcircuits. Especially for high power microcircuits, i.e. insulated gate bipolar transistor (IGBT), high temperature, induced by heat flow, will cause parameter drifting or even failures. Numerous researches have been conducted on die-attach layer or its inner defects. Within the researches, the size [1,2], position [3], pattern [4], and even depth [5] of the die-attach defects have been discussed, and their influences on thermal [6], mechanical [7,8] and parameter-stable [9,10] performance have been also studied. In most of those researches, heat sources have been treated as an entity. However, the heat generation distribution affects thermal analysis results at the same time. Hot spots may be concealed by the assumption of uniform heating. For devices composed of plentiful repetition units, i.e. IGBTs or memories, the distribution of heat sources is also determined by the operating mode [11,12].

Meanwhile, current thermal analyses of devices are mainly based on equivalent thermal resistance network or finite element (FE) method [13–15]. No matter which method is employed, dissipation factors, including material property, dimension parameter, power distribution and boundary condition, should be determined in advance. The precision of the thermal analysis depends on the accuracy of the factors set in the analysis models to a great extent, which may be difficult to acquire sometimes. For example, the heat conductivity of the die-attach depends on both the material and the process, which will vary with each individual, especially in the case of porous die-attach pastes [16,17]. At the same time, whenever the operating mode switches, the analysis models have to be modified or rebuilt correspondingly, which will also increase the modeling work.

To cope with the problems, an approach that could simplify the thermal analysis of chips with variable power will be proposed in this paper. With this approach, the steady temperature distribution could be acquired only with the information of power distribution

* Corresponding author.
E-mail address: pigeonzn@126.com (C. Pei).

http://dx.doi.org/10.1016/j.applthermaleng.2017.04.010
1359-4311/© 2017 Elsevier Ltd. All rights reserved.

in different operating modes and the example temperature measurement result. The paper is arranged as below. Firstly, the theory of the simplified approach will be introduced. Subsequently, a series of typical power distributions will be given, and their thermal influences will be solved by the FE method and the proposed approach. Their temperature distributions will be compared to verify the accuracy of the approach. Meanwhile, the relationship between the undetermined coefficients and other dissipation factors will be discussed. Finally, a case study will be given. The steady temperature distribution measured by infrared microscopy and the analytical result based on this approach will be compared again to verify the approach.

2. Theory & methodology

The typical heat dissipation route for encapsulated chips is illustrated in Fig. 1(a). As to the low heat conductivity of thermal molding compound, most of heat dissipates from the die-attach layer through the carrier to the mounting plane or the heat sink [18]. In a simplified form, the temperature of chip is determined by power distribution, power intensity, material thermal properties and boundary conditions, as Fig. 1(a) shows. In this paper, spatial analysis is utilized to depict the power distribution and identify the influence, which has been employed in other works on defect detection [19,20] or condition evaluation [21]. Among spatial analysis methods, spatial autocorrelation method, proposed by A. D. Cliff and J. K. Ord [22] in 1980s, is most promising and has been applied to wafer defect detection [23]. In these studies, the defective dies, fabricated on a single wafer, were summed as a wafer map to display the spatial dependence across the wafer. Based on it, spatial autocorrelation was extracted and spatial effect could be resolved. Similar to wafer map, chips with variable power will be also meshed into matrix-arranged lattices in this paper, as Fig. 2 illustrates. Let matrix $M_{a,b}$ denote the chip. The power of unit (i, j) is expressed as $X\,(i, j)$.

The definition of the power of each unit is:

$$X(i,j) = \begin{cases} 1, \text{work} \\ 0, \text{non}-\text{work} \end{cases} \quad (1)$$

For simplification, the power of each unit is assumed to be equal and $X_{a,b}$ is transformed into a 0–1 matrix. The distance was measured by counting the minimum steps between two units. In other words, the heat is only permitted to transfer between adjacent units. For any unit (h, i) and any other unit (j, k), their distance could be expressed as:

$$d_{h,i}(j,k) = |h-j| + |i-k| \quad (2)$$

For unit (h, i), the units at d distance are separately summed as:

$$W^0_{h,i}(g) = \{X(j,k)|d_{h,i}(j,k) = g, X(j,k) = 0, g \geqslant 1\} \quad (3)$$

$$W^1_{h,i}(g) = \{X(j,k)|d_{h,i}(j,k) = g, X(j,k) = 1, g \geqslant 1\} \quad (4)$$

$$H^1_{h,i}(g) = |W^1_{h,i}(g)| \quad (5)$$

$|\cdot|$ in Eq. (5) denotes the total number of set elements. Particularly, $H_{h,i}(0)$ denotes the operating condition of unit (h, i) itself.

According to Fourier's law, the temperature rise of units is dependent on the thermal resistance, heat generation, and boundary heat flux. For each unit in the chip, excepting the heat generated interiorly and the heat flow exteriorly the chip bottom, the heat inflow (or outflow) from neighboring units should also be considered. Actually, the hot spots appear not only in the area with high heat intensity but also in the operation units "crowded" area. According to the first law of geography, "everything is related to everything else, but near things are more related than distant things" [24], the synergy influences between units should be considered and converge with distance. The simplified equivalent circuit of the dissipation route is illustrated in Fig. 1(b). According to superposition theorem, if temperature variation is limited and the thermal material properties remain stable, the steady temperature rise of the chip could be expressed as the linear superposition of influences of all heat sources (or operating units). Based on the hypothesis, the steady temperature matrix $T_{a,b}$ could be expressed as below:

$$T = AZ + B \quad (6)$$

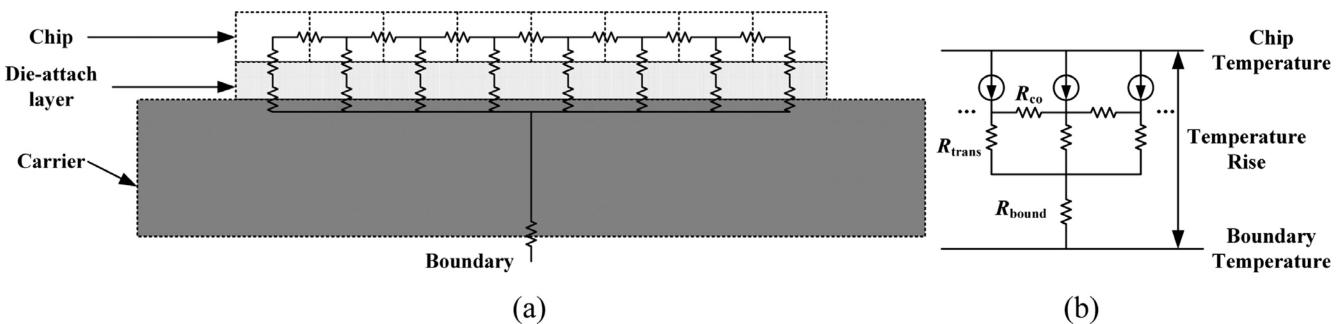

Fig. 1. Dissipation route and equivalent circuit: (a) Typical dissipation route for encapsulated chips (b) the simplified equivalent circuit.

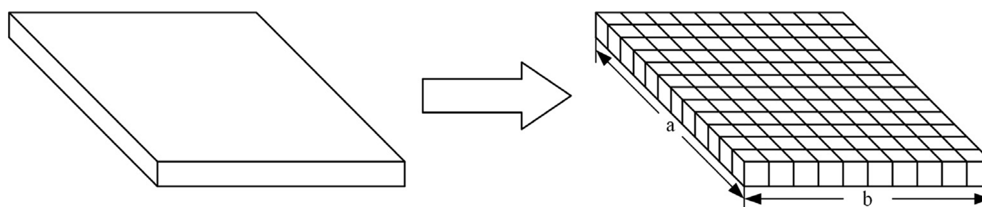

Fig. 2. Chip meshed into matrix-arranged lattices.

Download English Version:

https://daneshyari.com/en/article/4991013

Download Persian Version:

https://daneshyari.com/article/4991013

Daneshyari.com