Correlation of Gate Capacitance with Drive Current and Transconductance in Negative Capacitance Ge PFETs

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***Abstract*— Correlation of gate capacitance C_G with drive current I_{DS} and transconductance G_m in negative capacitance (NC) Ge pFETs is first investigated. Hysteresis-free NC Ge pFETs integrated with 4.5-nm HZO achieving the improved I_{DS} and G_m over the control devices are fabricated. A peak in the C_G versus gate voltage curve is demonstrated in the NC Ge pFET, indicating the NC effect induced by HZO film. It is observed that I_{DS} and G_m of the NC transistors are enhanced as the C_G peak gets increased. This is attributed to the fact that, as the device operates in the NC region, both C_G and internal gate voltage amplification are proportional to $C_{FE}/(C_{FE} + C_{MOS})$, where C_{FE} and C_{MOS} are the NC of HZO and the MOS capacitance of the device, respectively.**

***Index Terms*— Negative capacitance, ferroelectric, germanium, Ge, transistor, FET, subthreshold swing.**

I. Introduction

NEGATIVE capacitance (NC) field-effect transistor (FET) is considered as the promising candidate for the energy-efficient logic switching applications, due to its ability for breaking through the Boltzmann limit [1]. Great research effort has been devoted to exploring the NC transistors with subthreshold swing (SS) below 60 mV/decade characteristics [2]–[7].

In the previous work, we realized the NC Ge(Sn) pFET integrated with 6.6 nm HZO [6]. Although the NC devices obtained steep sub-60 mV/decade SS, and improved drive current I_{DS} over conventional control device without HZO, the undesirable hysteresis occurred. The calculation showed that the hysteresis of NC transistor can be effectively eliminated by reducing the thickness of ferroelectric film [8]. According to the recent theoretical works [9], [10], the peaks in gate capacitance C_G with V_{GS} for the NC Ge(Sn) FETs in [6] also can prove the NC effect. However, the relationship between C_G characteristics and electrical performance in NC transistors remains unclarified.

In this letter, the hysteresis-free NC Ge pFETs with the improved I_{DS} and transconductance G_m over the control devices without HZO are demonstrated. We report the first investigation of correlation between C_G and I_{DS} as well as that between C_G and G_m in the NC Ge transistors.

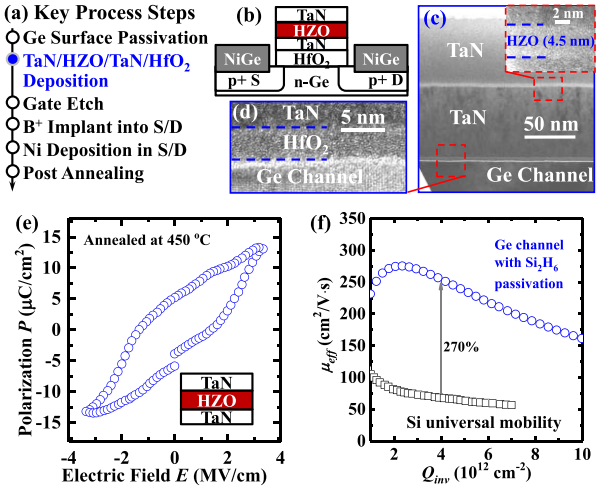

Fig. 1. (a) Key process steps for the fabrication of ferroelectric NC Ge pFETs. (b) Schematic of fabricated NC Ge transistor. (c) TEM image shows the gate stack of the NC transistor on Ge. The inset illustrates that the thickness of HZO is 4.5 nm. (d) HRTEM image features TaN/HfO_2 on Ge channel. (e) Measured *P-E* loop for a TaN/HZO/TaN sample annealed at 450 °C, confirming the ferroelectric phase of HZO. (f) Plot of μ_{eff} versus Q_{inv} extracted from the Ge control pFETs showing that Ge achieves a 270% improvement in μ_{eff} at a Q_{inv} of 4×10^{12} cm^{-2} over Si.

II. Device Fabrication

Key process steps for NC Ge pFETs fabrication are shown in Fig. 1(a). Ge surface was passivated using Si_2H_6, and then TaN/HZO/TaN/HfO_2 stack was deposited. HZO with thickness of 4.5 nm was utilized. After gate etch, source/ drain (S/D) regions were implanted with boron (B^+) and non-self-aligned

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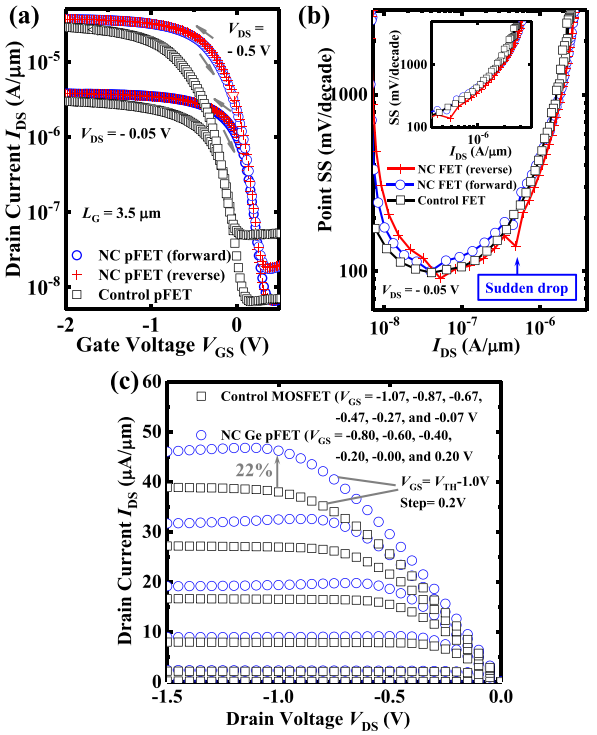

Fig. 2. (a) Measured I_{DS}-V_{GS} curves of a pair of ferroelectric NC Ge pFET and control device annealed at 450 °C. (b) Point SS versus I_{DS} characteristics showing the sudden drop in some points of SS of NC transistor. (c) I_{DS}-V_{DS} curves of the devices. A 22% I_{DS} improvement is achieved in the NC Ge pFET compared to the control device at a supply voltage of − 1.0 V.

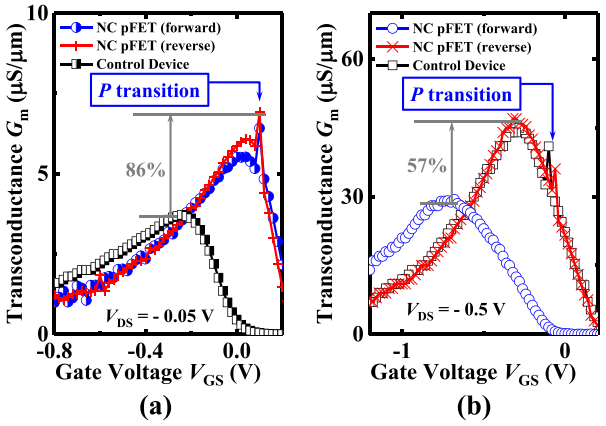

Fig. 3. G_m as a function of V_{GS} curves of the NC Ge pFET and the control device measured at V_{DS} of (a) − 0.05 V and (b) − 0.5 V. Significant enhancement in G_m is achieved in NC transistor over the control device. G_m peaks resulted from the P transition in HZO are observed in NC transistor.

Ni was formed in S/D regions. Finally, a post annealing for 30s was carried out at 450 °C for dopant activation, S/D metallization and crystallization of HZO film. Ge control pMOSFETs without HZO were also fabricated.

Fig. 1(b) shows the schematic of the fabricated NC Ge pFET. TEM image in Fig. 1(c) shows the TaN/HZO/TaN/HfO_2 stack on Ge. The inset illustrates that the thickness of HZO is 4.5 nm. HRTEM image in Fig. 1(d) presents the HZO dielectric on passivated Ge channel. Fig. 1(e) shows the measured curve of polarization P as a function of electric filed E for a TaN/HZO/TaN sample annealed at 450 °C, and the ferroelectric phase is confirmed by the P-E hysteresis loop. Fig. 1(e) illustrates the effect mobility μ_{eff} as a function of inversion charge density Q_{inv} in the Ge channel region extracted based on a total resistance slope-based approach from Ge control pFETs [11]. μ_{eff} values are consistent with those of relaxed Ge pFET in [12]. It is noted that μ_{eff} is not dependent on the TaN thickness, indicating that no stress is introduced into channel by metal gate. The S/D resistance $R_{S/D}$ extracted using control devices is about 4 kΩ · μm, which is assumed to be the same as that of NC transistors due to the same S/D process steps.

III. Results and Discussion

Fig. 2(a) shows the measured transfer characteristics of a pair of ferroelectric NC Ge pFET and control device without HZO at the V_{DS} of −0.05 V and −0.5 V. The devices underwent a post annealing at 450 °C, and have a gate length L_G of 3.5 μm. Hysteresis-free I_{DS}-V_{GS} curves with forward and reverse sweeping indicated by arrows are demonstrated in the NC Ge pFET [Fig. 2(a)]. The NC transistor achieves the improved I_{DS} compared to the control device. Point SS versus I_{DS} curves in Fig. 2(b) show that the NC transistor exhibits the sudden drop in some points of SS of NC transistor. It is observed that after the sudden drop points, NC pFET achieves the improved SS compared to the control device. Fig. 2(c) shows the measured output characteristics of the same pair of devices. A 22% I_{DS} improvement is achieved in NC Ge pFET compared to the control device at $|V_{GS} - V_{TH}| = |V_{DS}| = 1.0$ V. Here, the V_{TH} is defined as the V_{GS} at I_{DS} of 10^{-7} A/μm at V_{DS} of −0.05 V. The V_{TH} values of NC pFET and control device are 0.20 and − 0.07 V, respectively. The higher I_{DS} in NC device is attributed to the NC effect due to the same μ_{eff} and $R_{S/D}$ of the two transistors. I_{DS}-V_{DS} curves of the NC transistor show the obvious NDR phenomenon, which is a typical characteristic of NC transistors [13]–[15]. The NDR phenomenon is attributed to the fact that, although V_{GS} is held a constant, the voltage drop at HZO is affected by the V_{DS}. During the measurement of I_{DS}-V_{DS} curves with the fixed V_{GS}, the increasing of V_{DS} leads to the reduction of charge in internal gate, due to the drain-to-channel coupling. This will cause the decreasing of the voltage drop at HZO. Its NC effect results in the reduced inversion charge density in channel and I_{DS} [13].

G_m as a function of V_{GS} curves of the NC transistor and control device at V_{DS} of −0.05 V and −0.5 V are illustrated in Fig. 3. NC Ge pFET obtains the significantly improved G_m over the control device. At V_{DS} of − 0.05 V and −0.5 V, 86% and 57% enhancement in maximum G_m are achieved in NC transistor, respectively, in comparison with that of control device. Whether forward or reverse sweeping V_{GS} configuration is employed, the obvious peaks in the G_m versus V_{GS} curves are observed in the NC Ge pFET at various V_{DS}, which was also detected in [6]. It is noted that, at the fixed V_{DS},