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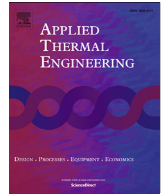

Research Paper

An effective and efficient numerical method for thermal management in 3D stacked integrated circuits

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HIGHLIGHTS

- A fast and accurate equivalent approach for thermal management was proposed.
- The efficiency of proposed model outperformed the detailed FE model with comparable accuracy.
- Presenting the effects of structural and material parameters on steady-state temperature profiles.
- The SiO_2 layer significantly affects temperature distribution in TSV interposer/chips.
- Junction temperature of 3D stacked ICs highly depends on heat source settings.

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ABSTRACT

Three dimensional (3D) integration technology has emerged as a promising solution to improve the performance of microelectronic devices. However, the complex structures and the consequent increase in power density exacerbate the challenge of thermal management in the device with multiple chips. Thus, an effective thermal analysis method is crucial for the reliability of 3D IC device. In this paper, a fast and accurate equivalent approach based on finite element analysis (FEA) was proposed for estimating the equivalent thermal conductivity of 3D IC device, and the proposed numerical model was validated by 3D FEA method. In addition, the estimated equivalent thermal conductivity was employed in thermal analysis of real 3D IC device, whose efficiency significantly outperformed the conventional detailed FE model with comparable accuracy. Furthermore, the effect of the structure and material related parameters on steady-state temperature profiles in 3D stacked packages has been systematically analyzed, including the diameter and pitch of TSVs, the thickness of SiO_2, the heat source setting as well as underfill materials, which provides useful insights for thermal management in 3D IC industry.

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1. Introduction

Three dimensional integrated circuits (3D ICs), one of the promising technologies to achieve smaller, thinner, and lighter products, overcomes the bottleneck of interconnects in the advanced nanoscale Integrated Circuit (IC), which reduces power consumption and improves the performance of the system with shorter vertical paths for connection based on through-silicon vias (TSVs) as well as providing higher bandwidth between heterogeneous chips without relying on further device scaling [1–4]. However, with respect to conventional two dimensional (2D) integrated circuits, it also exacerbates the challenge of thermal management in 3D stacked ICs duo to the higher power densities and the increase in the number of stacked dies, together with the use of interfacial layers with poor thermal conductivity [5–8]. Unfortunately, thermal problems increase the degradation of the performance and reliability of 3D stacked electronic systems. Specifically, higher temperature decreases lifetime and reduces the performance [9,10]. Furthermore, large temperature gradient creates significant thermal stress, potentially resulting in prominent thermal–mechanical reliability issues, such as solder interconnect fatigue failure, substrate delamination and die cracking [11,12]. Therefore, heat and thermal related analysis is imperative for determining the practical applicability of 3D technology and evaluating various 3D design options.

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Nomenclature

l_{Cu} width of copper layer in equivalent model, m
t_{SiO_2} thickness of SiO_2 layer in equivalent model, m
d diameter of copper filled TSV, m
d_{SiO_2} external diameter of SiO_2 layer, m
$K_{x,y}$ equivalent thermal conductivity of TSV interposer/chip in-plane direction, W/(m K)
K_z equivalent thermal conductivity of TSV interposer/chip in cross-plane direction, W/(m K)
q_x heat flux on the x orientation, J/(m^2 s)
q_z heat flux on the z orientation, J/(m^2 s)
Δz length in z orientation between two cross sections, m
Δx length in x orientation between two cross sections, m
ΔT_x average temperature difference between cross section 1 and 2 in x direction, K
ΔT_z average temperature difference between cross section 1 and 2 in x direction, K
$K_{eq,x\text{-}y}$ equivalent thermal conductivity of micro-bump in in-plane direction, W/(m K)
$K_{eq,z}$ equivalent thermal conductivity of micro-bump in cross-plane direction, W/(m K)
k_n thermal conductivity of the *nth* material in micro-bump, W/(m K)
v_n volume fraction of the *nth* material in micro-bump

Abbreviations
3D three dimensional
2D two dimensional
IC integrated circuit
FC flip-chip
FEA finite element analysis
FE finite element
TSV through silicon via
SiO_2 silicon dioxide
IMC intermetallic compound
CFD computational fluid dynamics
CPU central processing unit
DRAM dynamic random access memory
CMOS complementary metal oxide semiconductor
EMA effective medium theory
HBM high bandwidth memory
UBM under bump metallurgy

To evaluate and optimize the heat dissipation performance of electronic products, various thermal measurement methods were proposed by researches. One way in which hardware designers have tried to address the thermal problem is with the use of thermal-aware floor planners [13]. Moreover, experimental methods such as thermal test die [14], thermocouples [15], infrared thermography [14]and Raman spectroscopy [16], have been extensively established and used in 3D ICs thermal management. However, thermal infrared system offers limited resolution of substrate thermal profiles and is not suitable for 3D designs with multiple layers. Similarly, the number of thermocouples and integrated thermal sensors are limited due to the routing and pin-out constraints. Most importantly, these experimental methods can only provide thermal profiles after fabrication that is not practical for optimization at early design stage.

By contrast, numerical method is widely applied in predicting the temperature profile in 3D ICs. In literature, many researchers have extensively employed a variety of numerical methods for thermal management. For example, thermal performance of 3D IC integration was investigated based on both 3D FEA and computational fluid dynamics (CFD) analysis, where analytical models for thermal conductivities of the interposer in-plane and cross-plane by considering various parameters was developed [17]. The heat dissipation capability of complementary metal oxide semiconductor (CMOS) image sensor with high-density TSVs under natural convection was evaluated through FEA and rule-of-mixture [18]. Wang et al. proposed a procedure for deriving equivalent thermal conductivities of complex materials as composites by the five basic structural models, i.e., Series, Parallel, two forms of Maxwell–Eucken, and Effective Medium Theory (EMA), using simple combinatory rules based on structure volume fractions [19,20]. In addition, thermal resistance network model based thermal equivalent of TSVs was proposed, and the transient thermal analysis of interconnect structure was investigated based on 3D thermal circuit RC transmission line model [21,22]. Meanwhile, two-dimensional model was proposed to predict equivalent thermal conductivity in the TSV chips [23]. However, these proposed methods either aimed for basic structure or significantly simplified the actual structure to achieve feasibility. More specifically, 3D FEA for interposer/chip is complex and time consuming due to the large number of multiple scale TSV structure, which lead to the detailed 3D numerical computation infeasible in personal computer or small workstation, and most of numerical methods ignored the dielectric layer-silicon dioxide (SiO_2) in the TSV interposer/chip, thereby leading to a lack of practical feasibility. Nevertheless, the SiO_2 layer was confirmed to play a significant role in the thermal behaviors of the TSV interposer/chip [18]. Unfortunately, the current two-dimensional model is not suitable when the SiO_2 layer was considered. Given the actual 3D IC devices containing heterogeneous material and multiple scale structure, an effective and efficient method is required to obtain the temperature profile in 3D IC which is helpful for thermal management and power dissipation understanding in advanced IC devices towards high reliability applications. In addition, the effective approach also provided a strong foundation for developing hierarchical multi-scale model, which is a combination of atomistic and continuum method, based homogenized representative volume elements.

In this work, a two-dimensional equivalent anisotropic thermal conductivity model was presented to simulate the thermal behavior of the TSV interposer/chip with various parameters, such as TSV diameters, pitches, and SiO_2 layer thickness. In order to improve computational efficiency while still maintaining computational accuracy, the TSV interposer/chip and micro-bump were homogenized as an effective medium to overcome the complexity of thermal analysis of the 3D stacked ICs. More specifically, heterogeneous TSV interposer/chip was modeled as a vertical homogeneous and horizontal anisotropic material. The SiO_2 layer in the TSV interposer/chip and intermetallic compound (IMC) layers in the micro-bump were considered to numerically estimate equivalent anisotropic thermal conductivity. Lastly, parametric analysis was performed to seek a design guideline for enhanced thermal performance in 3D ICs.

2. Computational and simulation models

3D thermal FE model was employed for evaluating the thermal distribution of the 3D stacked ICs under a steady-state natural convection condition. Since the 3D stacked packaging includes hetero-

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