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Natural convective boiling in horizontal and inclined micro-channels structure using super-moist fluids for cooling 3D stacked chip

Ping-yang Wang, Shuang-fei Li, Zhen-hua Liu *

School of Mechanical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China

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ABSTRACT

A novel micro-channels heat pipe technology which passively cools 3D chips was proposed. The micro-channels structure of 3D chips was used as the evaporating section of the heat pipe. The maximum heat flux and heat transfer coefficient of boiling in horizontal and inclined micro-channels were studied experimentally studied. Experiments were carried out using four kinds of working liquids: two pure fluids (deionized water and R113) and two super-moist fluids (deionized water + surfactant and R113 + surfactant). The height and gap of channels used were in the range of 30–90 mm and 30–100 μm, respectively. Experimental results show that horizontal and inclined micro-channels structure can also cause great natural convective boiling to cool 3D chip, simultaneously, super-moist fluids can significantly enhance both the maximum heat flux and heat transfer coefficient of boiling in micro-channels due to super-wettability of the liquids. The results show that the horizontal micro channel heat pipe structure is also a promising technology for 3D chip cooling.

1. Introduction

With the development of electric technology, 3D chip has been considered as a new chip integration technology in which chips are no longer connected side by side, but the upper and lower parallel connection. Researches have shown that the length of global wires can be reduced by as much as 50% in 3D chip [1]. 3D integration technology is also considered as the preferred option to achieve miniaturization. However, the higher integration degree of 3D chip will lead to more power consumption per unit area of the chip. If the heat emitted by the chip cannot be dissipated in time, it will result in temperature excursion, which not only affects the normal operation of the computer, but also reduces the longevity of the chip. Long term reliability drops by 50% for each 10 degree rise in junction temperature [2].

For 2D chip cooling, many studies have proposed various cooling methods [3–7], from the initial air, water cooling to heat pipe, micro-channels, micro-refrigeration systems, etc. Some special physical phenomena such as semiconductor, thermionic, thermoacoustic are also developed for 2D chip cooling. Micro-channel cooling methods for 2D chip is a rapidly developing cooling technology in recent years that was firstly proposed by Tucherman and Peace [8] in 1981. Up to now, studies of micro-channel cooling have been either single-phase forced convection or forced convection boiling. The working fluid driven by external power is forced to flow through micro-channels mounted in the substrate to absorb heat from chips. Micro-channels have large surface area, and fluid in the channels has a thin boundary layer, resulting in high heat transfer coefficient (HTC). Whether it is forced convection or boiling flow, the cooling capacity of micro-channels is much larger than traditional water-cooling method. The size of micro-channels varies from a few microns to several millimeters, and cooling capacity is also different for different structures.

Different from traditional 2D chip, 3D chip cooling cannot simply use the cooling channels mounted in the substrate due to that horizontal chips are stacked in vertical direction and the adjacent gaps are as small as a few microns, which cause great difficulty for intermediate chip cooling and temperature limitation [9]. Therefore, large-scale development of 3D stacked chips need low-cost and high efficiency cooling solution. The current prototype 3D chip is still in the development stage, and there is no commercial application yet. 3D chip cooling technology is an extension of 2D chip, and it is in the stage of raise of conceptions and numerical simulations. Only a few experimental studies were published. Up to now, most of the 3D stacked chip's cooling design conceptions have been active methods that micro-channels are installed in encapsulation, and working fluid driven by external power flows through the micro-channels to take away heat.

* Corresponding author.
E-mail address: liuzhenh@sjtu.edu.cn (Z.-h. Liu).

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Nomenclature

b	width of channel (m)
d	gap of channel (m)
D_e	hydrodynamic equivalent diameter (m)
f	friction coefficient
g	local acceleration of gravity (m/s^2)
H	height of the horizontal channel center to liquid level (m)
h	heat transfer coefficient (W/(m^2 · K))
H_{fg}	latent heat of evaporation (J/kg)
L	length of channel (m)
I	electric current (A)
p	pressure (Pa)
P	power (W)
q	heat flux (W/m^2)
q''	critical heat flux (W/m^2)
S	surface area (m^2)
t	temperature (°C)
$\Delta\overline{T}$	mean superheating (K)
U	voltage (V)

Greek letters

Φ	dimensionless heat flux
θ	inclined angle of channel
β	contact angle (°)
ρ	density (kg/m^3)
μ	dynamic viscosity (Pa · s)
υ	specific volume (m^3/kg)
σ	surface tension coefficient (N/m)
τ	frictional shear stress (Pa)

Subscripts

0	pure liquid
buo	buoyancy
cap	capillarity
h	horizontal
v	vertical or vapor phase
l	liquid phase
m	mean value
s	saturated state or SDS
w	heating surface
loss	heat loss
θ	inclined angle of channels

Kandlikar [10] proposed a review and projections of integrated cooling systems for three-dimensional integrated circuits in the last decade and provides a vision for codesigning 3D IC architecture and integrated cooling systems.

Poulikakos and co-workers [11] performed a simulation work to develop a multiscale conjugate heat transfer model for integrated water cooling of chip layers and validated with experimental measurements on an especially designed thermal test device that simulates a four tier chip stack. The model is used to predict the behavior of multilayer stacks when the heat flux changes due to the variations of computational load of the chips.

Matsumoto, Mori and Orii [12] carried out a thermal performance evaluation of dual-side cooling for a three-dimensional chip stack. They described how to realize effective cooling from the bottom side of chips, which consisted of organic dielectric materials and copper as substrate.

Shamim and co-workers [13] presented an energy efficient wireless 3D NoC architectures with optimal dimensions of microchannels for best thermal cooling capability and pressure characteristics by making the vertical interconnects across the cooling layers with on-chip wireless interconnects.

Tan et al. [14] designed a single phase liquid micro-channel cooling solution to overcome the problem of intermediate stacks cooling. A dual inlet, dual outlet micro-channel heat sink with a supply plenum tapering downstream was used to provide an even flow distribution, obtaining lower thermal resistance and lower temperature variation on the die.

Kim and Kim [15] designed a micro flat heat pipe system (MFHP) for cooling a self-convectional three-dimensional integrated circuit. The electro thermal behavior of the structure was modeled by an equivalent circuit for simulation. Experimental measurements demonstrated that the temperature of the chip under test drops about 42 °C by using the MFHP on the chip in steady state. The cooling performance of the proposed system is satisfactory for 3D IC cooling system on mobile applications.

Furtherly, Koo and co-workers [16] performed a study on integrated microchannel cooling for three-dimensional electronic circuit architectures. Mizunuma, Yang and Lu [17] developed a thermal model for analyzing thermal performance of 3D-ICs with integrated microchannel cooling. Feng and Li [18] carried out also a fast thermal analysis on CPU for 3D ICs with integrated microchannel cooling. Sridhar et al. [19] proposed a compact thermal model, and simulations were performed to compare to the experimental data. Khan et al. [20] conducted an experimental research on a cooling method for 3-D packaging with through-silicon via (TSV) for electrical and fluidic interconnections. However, these active type methods have several drawbacks, such as complex internal structure of encapsulation with micro-channels inside, manufacture difficulties, additional power components, and fluid leakage. Therefore, active type cooling methods of 3D chips are still very difficult for actual application.

Recently, the authors presented a new conception for passive 3D chip cooling and carried out a preliminary experiment [21]. A vertical micro-scale thermosyphon heat pipe structure was designed for 3D chip. This heat pipe structure utilizes 3D chip's specific micro structure to form a thermosyphon boiling with the driving force of the combination of buoyancy and capillarity. In general, conventional 3D stacked chip encapsulation is placed horizontally. But if it is deliberately arranged vertically, tens of microns gap between chips can form vertical micro-channels with two open ends. According to this geometrical characteristic, insulating liquid is filled in the lower half of the encapsulation and submerges the 3D stacked chips, and then the vertical micro-channels among vertical chips submerged in saturated liquid would form the evaporating section of a micro-scale thermosyphon heat pipe. The upper surface of the encapsulation can be processed as heat sink for condensation. Saturated liquid flows upward along micro-channels and absorbs heat generated by chips in micro-channels, then evaporates into saturated steam gradually, discharged from the upper outlet of the channels continuously under buoyancy and capillarity. This heat transfer mode is generally called thermosyphon boiling. The steam rises to the upper surface of the encapsulation and is condensed by cooling fluid flowing through the heat sink, thereby completing a heat pipe working cycle. Based on the experimental results, it is found that vertical thermosyphon heat pipe utilizing 3D chip's specific micro struc-