International Journal of Heat and Mass Transfer 108 (2017) 210–219

Contents lists available at ScienceDirect

International Journal of Heat and Mass Transfer

journal homepage: www.elsevier.com/locate/ijhmt

Heat source layout optimization in two-dimensional heat conduction using simulated annealing method

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ARTICLE INFO

Article history:
Received 19 July 2016
Received in revised form 19 October 2016
Accepted 4 December 2016

Keywords:
Heat source layout
Heat conduction optimization
Simulated annealing method
Bionic optimization

ABSTRACT

Heat source layout optimization is an effective way to enhance heat transfer for electronic cooling. In this paper, the heat source layout optimization in two-dimensional heat conduction is investigated using simulated annealing (SA) method. Mathematical analysis is conducted to transform the heat source layout problem into a combinatorial optimization problem, which can be solved by SA. Three typical cases with various boundary conditions are introduced to validate the effectiveness of SA for heat source layout optimization. The solutions of SA are compared to the ones of random distribution (RD) and the ones of bionic optimization (BO). The results indicate that the maximum temperature of the domain can be remarkably reduced after optimizing the heat source layout using SA compared to RD. Compared to BO, it needs more computational time for SA to obtain the solution. Furthermore, the maximum temperature after optimizing by BO is lower than the ones by SA for the cases with symmetric boundary conditions. While for the case with asymmetric boundary conditions, SA performs better and the maximum temperature lower than BO is obtained. It can be concluded that simulated annealing method is effective to optimize the heat source layout problem in heat conduction.

1. Introduction

In nowadays, the component integration of electronic devices increases the power density remarkably, which makes the cooling of electronic devices difficult. The maximum temperature of electronic devices is an important index that influences the performance and the service life of electronic equipment. Therefore, how to dissipate the generated heat as soon as possible and reduce the maximum temperature of electronic component have become a critical problem for the development of microelectronic technology.

The components in the electronics generate heat when working, which can be treated as heat sources. One effective method to enhance the heat dissipation performance of the electronics is to insert high thermal conductivity material into the domain. The inserted high thermal conductivity material reduces the local thermal resistance, obtaining a lower maximum temperature. Some approaches have be developed to arrange the distribution of the inserted material for heat transfer enhancement, including the constructal theory [1–9], the entransy theory [10–19], the bionic optimization [20–22] and the combinatorial algorithms [23–25]. Through these methods, a tree-shape high thermal conductivity channels were obtained, which can effectively reduce the maximum temperature of the domain. In recent years, some high thermal conductivity pathways with various fixed shapes are also introduced for heat conduction enhancement, such as X-shape [26,27], Fork-shape [28], Phi-shape and Psi-shape [29], V-shape [30], and Plus-shape [31]. In these studies, the influence of the width of the pathway on the heat transfer performance was discussed and the suggested value of the width was provided.

The configuration optimization of heat sources is another effective way to enhance the heat transfer and reduce the maximum temperature. Many efforts have been made for heat source layout optimization. Bejan et al. [32] used theoretical, numerical and experimental methods to study the influence of the space of horizontal cylinders in a fixed volume on the heat conduction performance with natural convection boundary condition. The dimensionless relations were provided to predict the optimal space. Stanescu et al. [33] studied the similar problem with forced convection boundary condition. The study also gave an approximated dimensionless relations to predict the optimal space of the

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http://dx.doi.org/10.1016/j.ijheatmasstransfer.2016.12.007
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Nomenclature

A_j	area of the *j*th grid cell, m^2
A_ϕ	total area of heat sources placed in the domain, m^2
$A_{\phi i}$	area of the *i*th heat source, m^2
D	distance that heat source can be moved during random walk, m
$D_{x,ij}, D_{y,ij}$	horizontal distance and vertical distance between the *i*th and *j*th heat sources, m
h	convective heat transfer coefficient, $W/(m^2 \cdot K)$
k	thermal conductivity, $W/(m \cdot K)$
l	side length of heat source, m
L	side length of domain, m
N_s	number of heat sources placed in the domain, 1
N_g	number of grid cells for placing heat sources, 1
N_{op}	number of temperature field calculations, 1
N_{lo}	number of loops during annealing process, 1
N_{anneal}	number of anneal steps, 1
N_{adjust}	times of heat source position adjustment, 1
R_x, R_y	uniform distributed random number within $[-0.5, 0.5]$, 1
R_{max}	dimensionless maximum temperature rise, 1
t	system annealing temperature, K
t_0	initial system annealing temperature, K
t_{te}	terminating system annealing temperature, K
T	temperature, K
T_0	environmental temperature, K
T_b	temperature before adding heat sources, K
T_i	temperature rise induced by the *i*th heat source, K
T_{max}	maximum temperature of domain, K
$\mathbf{U}$	uniform distribution random number within $[0, 1]$, 1
x, y	horizontal coordinate and vertical coordinate of domain, m
α	coefficient of annealing schedule, 1
ϕ_0	intensity of heat source, W/m^2
ϕ_b	heat source distribution before adding heat sources, W/m^2
ϕ_i	distribution of the *i*th heat source, W/m^2

horizontal cylinders in an array. Later Bejan demonstrated that the minimum peak temperature can be achieved through optimizing the space of the heat sources in a array [34]. Further studies indicated that the volume averaged heat transfer density can be increased through inserting additional heat sources into the current heat sources [35–40]. Chen et al. [41] investigated the influences of the distribution of heat sources on the cooling performance of a simulated electronic package experimentally. da Silva et al. [42] optimized the distribution of one-dimensional discrete heat sources on a wall with natural convection using constructal theory to maximize the global conductance. Nested loops method was used to obtain the optimal heat source layout with one, two and three heat sources, respectively. Later, the similar problems with different boundary conditions [43–45] and considering more practical situations [46–49] were also investigated. Subsequently, Hajmohammadi et al. explored the optimal arrangement of one, two, three and four two-dimensional heat sources surrounded with square-shaped fins [50] and circular-shaped fins [51], respectively. Several configuration styles of the heat sources were considered and the optimal characteristic distances of the configurations were obtained using constructal design to reduce the maximum temperature of the heat sources. The optimized results of the various heat source configuration were compared and discussed. Similarly, Gong et al. [52,53] and Feng et al. [54] optimized the heat source arrangement problem surrounded with cylindrical and helm-shaped fin under three-dimensional situations, respectively. The studies above mainly considered the heat layout optimization with small number of optimization degrees of freedom. For the problems with large number of degrees of freedom, combinatorial optimization algorithms are effective methods. Madadi and Balaji [55] determined the optimal layout of three heat sources under forced convection condition through using a micro genetic algorithm combining Artificial Neural Network (ANN). Sudhakar et al. [56] investigated the optimal positions of five discrete heat sources mounted on a wall of a three-dimensional vertical duct under mixed convection conditions using ANN. Soleimani et al. [57] used particle swarm optimization to optimize the positions of a pair of heat source-sink in an enclosure for the minimization of the maximum temperature. Hotta et al. [58,59] studied the configuration of five nonidentical heat sources mounted on a substrate board under mixed convection experimentally, and used a heuristic approach and an experiment driven ANN-GA based technology to optimize the configuration, respectively. In a recent study, Chen et al. [60] developed a bionic optimization for the heat source distribution problem in heat conduction, through which the maximum temperature of the domain can be reduced effectively.

In this paper, the heat source layout optimization in two-dimensional heat conduction is studied using simulated annealing method. Mathematical deduction is conducted to transform the problem to a combinatorial optimization problem. Then the combinatorial problem is solved using the simulated annealing method. Three typical cases with various boundary conditions are used to test the performance of simulated annealing method for heat source layout optimization. Comparison of optimized results and the ones by other methods in the previous studies is also conducted.

The remaining parts of the paper are organized as follows. Section 2 presents the mathematical models of the heat source layout optimization problem. Section 3 shows the mathematical analysis that transforms the problem to a combinatorial optimization problem, and the process of simulated annealing method are presented. Section 4 presents the results of three typical test cases and relevant discussion. Section 5 presents the conclusions.

2. Mathematical models

In this section, the mathematical models for the heat source layout optimization in two-dimensional heat conduction are introduced. The heat conduction domain is set as square and the boundary conditions are given. Several heat sources are added into the domain, which will increase the temperature of the domain. The optimization problem is to arrange the heat source layout to reduce the maximum temperature. Therefore, the objective is to minimize the maximum temperature of the domain, and the constraint is that the heat sources are not allowed to overlap with each other. The mathematical models for the heat conduction optimization problem is shown as follows.

$$\text{Objective} = \min(\max(T)) \tag{1}$$

s.t.

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right) + \sum_{i=1}^{N_s}\phi_i(x, y) = 0 \tag{2}$$

$$\text{Boundary}: \ T = T_0 \text{ or } k\frac{\partial T}{\partial \mathbf{n}} = 0 \text{ or } k\frac{\partial T}{\partial \mathbf{n}} = h(T - T_0) \tag{3}$$