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A modified bidirectional thermal resistance model for junction and phosphor temperature estimation in phosphor-converted light-emitting diodes

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Besides the junction temperature, phosphor temperature is another key parameter to characterize the thermal behavior of phosphor-converted light-emitting diodes (pc-LEDs). However, the measurement of phosphor temperature remains a challenge. In this paper, we proposed a modified bidirectional thermal resistance model for the junction and phosphor temperature estimation. Compared with the conventional thermal resistance model, both the heat generation of the phosphor layer and the heat flow through the phosphor layer were further considered in this model. Three LED packaging structures were fabricated and measured to complete the model. The heat generation of the chip and phosphor layer was measured. With varying driving current from 0.05 A to 0.65 A with an increment of 0.1 A, the maximum deviation of the predicted and measured junction and phosphor temperature is less than 1% and 9.2%, respectively, which proves the feasibility of the proposed model for the junction and phosphor temperature estimation.

1. Introduction

Light-emitting diodes (LEDs) are widely used in general lighting and flat-panel display applications with their advantages of high luminous efficiency, long lifetime and energy saving [1–3]. In order to realize the white light illumination, a yellow phosphor layer is coated on the blue LED chip to convert the blue light to yellow light, and then the converted yellow light mixes up with the transmitted blue light, and eventually generates white light [4–7]. Such a phosphor layer coated structure is called phosphor-converted LEDs (pc-LEDs). During the color conversion process in the phosphor layer, there exists optical energy loss including the Stokes shift loss, the non-unity quantum efficiency of phosphor particles and self-absorption of yellow light by the phosphors [8]. These optical energy loss is transformed into heat, which makes the phosphor layer another heat source in the pc-LEDs. Generally, the phosphor heat generation is quite small compared to the chip heat generation. Yan et al. revealed that about 8% of the input electrical power is converted into heat by the phosphors [9]. However, such small heat in the phosphor layer can also result in extremely high local temperature due to the low thermal conductivity of the phosphor/silicone composite. High phosphor temperature will reduce the quantum conversion efficiency of the phosphors and therefore lower the luminous efficiency [10]. Moreover, it induces the material property deterioration, local stress, and even delamination, which results in the degradation of reliability and lifetime of pc-LEDs significantly [11]. Luo et al. observed that the highest temperature of the phosphor particles can reach 315.9 °C, resulting in the phosphor quenching or even the silicone carbonization [12]. Therefore, besides the junction temperature, the phosphor temperature is also an important factor to characterize the thermal performance of white pc-LEDs.

However, the phosphor temperature is difficult to measure because the phosphor particles are dispersed in the silicone matrix and the phosphor diameter usually falls in the range of 13–15 μm. The measurement of phosphor temperature has remained a challenging problem for years. There was no experimental measurement of the phosphor temperature until Kim et al. attempted to directly measure the phosphor temperature by a micro thermocouple [13]. At such circumstance, developing alternative method to predict the phosphor temperature is meaningful and urgent.

Thermal resistance model is demonstrated to be an effective tool to predict junction temperature for LED packaging [14–17]. In the conventional model [14–16], it only takes into account of the heat dissipation path from the junction layer, to the heat slug, substrate, and the ambient. Chen et al. [18] proposed a bidirectional thermal resistance model considering the bidirectional heat

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flow on both sides of the LED packaging structure and improved the accuracy of junction temperature estimation. But they did not consider the heat generation of the phosphor layer in the model. Actually, for pc-LEDs, the heat produced in the phosphor layer cannot be ignored. To solve this problem, Juntunen et al. [19] developed an improved model and considered the heat generation of phosphor layer, but here they think both the heat from the phosphor and the chip transfers from the leadframe to the ambient. Additionally, their model only focused on junction temperature estimation and did not calculate phosphor temperature.

In this work, a modified bidirectional thermal resistance model considering both the heat generation of the phosphor layer and the heat flow through the phosphor layer is proposed to estimate the junction and phosphor temperature for pc-LEDs. Experimental measurements are conducted to validate the model.

2. Model establishment

The modified model is established based on the comparison of three LED packaging structures: (I) LED chip without coating, (II) with silicone coating, and (III) with phosphor coating (i.e., pc-LED), respectively, as shown in Fig. 1. Fig. 2 illustrates the schematic of the heat flow path and the corresponding thermal resistance model of these three packaging structures.

For LED chips without any coating, one-dimensional thermal resistance model is applied, as shown in Fig. 2(I). The LED packaging structure is simplified by neglecting the internal structure and only considering a bare chip attached to a substrate with die attach adhesive (DAA). Heat generated in the chip layer is transferred from the junction layer to the ambient through conduction and convection. In this case, the total junction-to-ambience thermal resistance $R_{1,j\text{-}a}$ is introduced to define the ratio of the temperature difference between junction temperature T_j and ambient temperature T_a, to the total heat flux Q_{chip}, which can be expressed as:

$$R_{1,j\text{-}a} = \frac{T_j - T_a}{Q_{chip}} \tag{1}$$

For LED chips with silicone coating, a bidirectional thermal resistance model is applied, as shown in Fig. 2(II). There are two heat transfer paths from the junction to the ambient, namely, the lower path and the upper path. The lower path refers to the conventional pathway which is from junction through substrate to the ambient and the corresponding thermal resistance is R_{j-s-a}. And the upper path is from the junction layer through silicone coating layer to the ambient and the corresponding thermal resistance is R_{sili}. In this way, the thermal resistance of the adding silicone layer R_{sili} is connected with R_{j-s-a} in parallel. It is noted that R_{j-s-a} can be regarded as equal to $R_{1,j-a}$ for the same series of LEDs. Knowing the total junction-to-ambience thermal resistance $R_{1,j-a}$ and $R_{2,j-a}$, we can calculate R_{sili} as:

$$R_{sili} = \frac{1}{1/R_{2,j-a} - 1/R_{1,j-a}} \tag{2}$$

For LED chip with phosphor coating, a modified bidirectional thermal resistance model is proposed, as shown in Fig. 2(III). Besides the chip heat generation Q_{chip}, there is another heat source, namely the phosphor heat generation Q_{phos}. In order to express the added heat source, it is necessary to introduce the phosphor node T_{ph} which is defined as the highest temperature in the phosphor layer. We assume that all the heat dissipation of phosphor layer is generated at the phosphor node. Then Q_{phos} is divided into two parts, namely, one is from the phosphor node to the ambient Q_{ph-a} through R_{ph-a}, and the other is from the phosphor node to the junction node Q_{ph-j} through R_{ph-j}. And the heat flux component Q_{ph-j} and Q_{chip} gather into Q_{j-a}, then continues conducting downward to the ambient node. Hence, there are three heat flow branches and the heat flux of each branch satisfies the following two equations:

$$Q_{ph-a} + Q_{ph-j} = Q_{phos} \tag{3}$$

$$Q_{ph-j} + Q_{chip} = Q_{j-a} \tag{4}$$

In order to calculate T_{ph}, we should firstly determine several parameters, including T_a, Q_{chip}, Q_{phos}, R_{j-s-a}, R_{ph-j} and R_{ph-a}. The ambient temperature T_a is usually a constant which can be measured easily. Q_{chip} and Q_{phos} can be calculated by the output optical power comparison between packaging structure (II) and (III). As for the thermal resistance R_{j-s-a}, R_{ph-j} and R_{ph-a}, indirect measurements can be applied to acquire these variables. Thermal transient tester (T3ster) is used for thermal characterization of those three packaging structures, of which the total junction-to-ambience thermal resistance is $R_{1,j-a}$, $R_{2,j-a}$ and $R_{3,j-a}$, respectively. We can assume that the thermal resistance from the junction through the substrate to the ambient R_{j-s-a} of three packaging structures are all approximately equal to $R_{1,j-a}$, which can be expressed as:

$$R_{1,j-s-a} = R_{2,j-s-a} = R_{3,j-s-a} = R_{1,j-a} \tag{5}$$

For packaging structure (II) and (III), the thermal resistance of the added coating can be regarded approximately as equal, as long as two conditions are satisfied, namely, one is that both the coating share the same morphology and the other is that the phosphor volume fraction is not too high so that the thermal conductivity difference between the silicone and phosphor coating is negligible. According to Yuan's work [20,21], thermal conductivity of the phosphor/silicone composite remains stable with a slight rise when phosphor volume fraction is below 40 vol.%. In this case, the following relationships are obtained:

$$R_{ph-j} + R_{ph-a} = R_{sili} \tag{6}$$

The next step is to solve the two variables R_{ph-j} and R_{ph-a}. Based on the proposed model, junction temperature T_j can be calculated as follows:

$$T_j = T_a + R_{1,j-a} \cdot Q_{j-a} \tag{7}$$

In addition, the difference between T_j and Ta can be calculated by the product of $R_{3,j-a}$ and the total heat generation of the

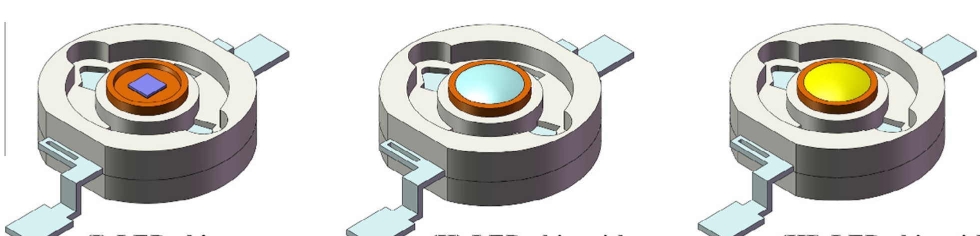

Fig. 1. Schematic of three LED packaging structures (I) LED chip without coating, (II) with silicone coating, and (III) with phosphor coating.