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Brief paper

Reachability and observability reduction for linear switched systems with constrained switching☆

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ABSTRACT

We present an algorithm for reducing the number of continuous states of a discrete time linear switched system, such that the reduced system has the same input–output behavior as the original system for a subset of switching sequences. The procedure can be interpreted as reachability and observability reduction for a linear switched system with constrained switching. The proposed method is expected to be useful for abstraction based control synthesis methods for hybrid systems.

1. Introduction

A discrete time linear switched system (Liberzon, 2003; Sun & Ge, 2005) (abbreviated by DTLSS) is a discrete time system of the form

$$\Sigma \begin{cases} x(t+1) = A_{\sigma(t)}x(t) + B_{\sigma(t)}u(t), \quad x(0) = x_0 \\ y(t) = C_{\sigma(t)}x(t), \end{cases} \tag{1}$$

where $t \in \mathbb{N}$ is the discrete time, $x(t) \in \mathbb{R}^n$ is the continuous state, $y(t) \in \mathbb{R}^p$ is the continuous output, $u(t) \in \mathbb{R}^m$ is the continuous input, $\sigma(t) \in Q = \{1, \ldots, D\}$, with $D > 0$, is the switching signal (discrete state), and the matrices A_q, B_q, C_q are of suitable dimension for $q \in Q$. A more rigorous definition of DTLSSs will be presented later on. For the purposes of this paper, $u(t)$ and $\sigma(t)$ will be viewed as externally generated signals. The present paper aims at providing a method to reduce the size of a DTLSS (that is, the number n) while preserving its input–output behavior for a set of switching sequences. This is achieved by eliminating those states which are not reachable and/or observable by switching sequences from the designated set. In the following, this problem will be called reachability/observability reduction for a DTLSS with constrained switching.

Motivating examples Besides its theoretical interest, the results are useful for control and analysis of switched and piecewise-affine systems.

(1) *Control and verification of DTLSSs with switching constraints.* DTLSSs with switching constraints occur naturally in a large number of applications. Such systems arise for example when the supervisory logic of the switching law is (partially) fixed. Note that verification or control synthesis of DTLSSs can be computationally demanding, especially if the properties or control objectives of interest are discrete (Aydin Gol, Ding, Lazar, & Belta, 2014). Even if the switching logic is not naturally fixed, for design purposes it might be reasonable to partially fix it in advance. Indeed, in that case the results of the paper can be used to replace the original model by a simpler one. Due to the high computational complexity of the existing control synthesis method, it might easily happen that it is impossible to synthesize a control law for the original model, but it is possible to do so for the reduced one. In that case, restricting the switching logic might help solving an otherwise intractable problem. The results of the paper could be useful for verification or control of such systems, if the properties of interest or the control objectives depend only on the input–output behavior. In this case, we could replace the original DTLSS Σ by the reduced (reachable and observable) DTLSS $\bar{\Sigma}$ whose input–output behavior for all the admissible switching sequences is the same

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as Σ. We can then perform verification or control synthesis for $\bar{\Sigma}$ instead of Σ. If $\bar{\Sigma}$ satisfies the desired input–output properties, then so does Σ. Likewise, if the composition of $\bar{\Sigma}$ with a controller meets the control objectives, then the composition of this controller with Σ meets them too.

(2) *Piecewise-affine hybrid systems*. Consider a piecewise-linear hybrid system H (Bemporad, Ferrari-Trecate, & Morari, 2000; van der Schaft & Schumacher, 2000). Such systems can often be modeled as a feedback interconnection of a linear switched system Σ of the form (1) with a discrete event generator ϕ, which generates the next discrete state based on the past discrete states and past outputs. As a consequence, the solutions of H correspond to the solutions $\{q_t, x_t, u_t, y_t\}_{t=0}^{\infty}$ of (1) with $q_t = \phi(\{y_s, q_s\}_{s=0}^{t-1})$. A simple example of such a system is $q_t = \phi(y_{t-1})$, $t > 0$, and q_0 is fixed, where ϕ is a piecewise affine map. Often, it is desired to verify if the system is *safe*, i.e., if the sequences of discrete modes generated by the system H belong to a certain set of safe sequences L for continuous input signals. Consider now another piecewise-affine hybrid system $\bar{H}$ obtained by interconnecting the discrete event generator ϕ with a reduced order DTLSS $\bar{\Sigma}$, such that the input–output behavior of $\bar{\Sigma}$ coincides with that of Σ for all the switching sequences from L. If L is prefix closed (see Notation 3), then H is safe if and only if $\bar{H}$ is safe, and hence, it is sufficient to perform safety analysis of $\bar{H}$. Since the number of continuous-states of $\bar{H}$ is smaller than that of H, it is easier to do verification for $\bar{H}$ than for the original model. Note that verification of piecewise-affine hybrid systems has high (in certain cases exponential) computational complexity, Frehse (2008) and Yordanov and Belta (2010). Likewise, suppose that it is desired to design a control law for H which ensures that the switching signal generated by the closed-loop system belongs to a certain prefix closed set L. Such problems arise in various settings when hybrid systems are modeled with discrete abstractions (Tabuada, 2009). Again, this problem is solvable for H if and only if it is solvable for $\bar{H}$, and the controller which solves this problem for $\bar{H}$ also solves it for H.

In Section 5, the results of the paper are illustrated on an example of verification for piecewise affine systems. A well established software package (FaPAS Yordanov & Belta, 2010) is used to check the results. It turns out that the software cannot verify the original model due to the computational expense; whereas, after the application of model reduction with the method given in the present paper, the software completes the verification task easily. For this example, a case study for control synthesis is also included on http://kom.aau.dk/~raf/Codes/Automatica2016. It is left out of the paper due to lack of space. An additional real world inspired example on power converter model order reduction is also included. In this example, the restriction on the allowed discrete mode sequences is imposed by the physical nature of the problem.

Related work The current paper is partially based on Bastug, Petreczky, Wisniewski, and Leth (2014). The main difference lies in the presence of detailed proofs and a clear system theoretic interpretation of the algorithms. Moreover, the algorithms of this paper yield DTLSSs which have the same input–output behavior *along* switching sequences from the designated set; as opposed to the same output response at the end of each allowed switching sequence. In Bastug, Petreczky, Wisniewski, and Leth (2016), a similar method is proposed for model reduction of continuous-time linear switched systems with respect to one specific switching sequence. However, the method in Bastug et al. (2016) is not stated for a set of switching sequences, and reachability/observability properties of the approximation system are again unknown. Some results on realization theory of linear switched systems with constrained switching appeared in Petreczky (2011). However, Petreczky (2011) does not yield a reachability or observability reduction algorithm. The subject of model reduction for hybrid and switched systems was addressed in many papers (Birouche, Guilet, Mourillon, & Basset, 2010; Chahlaoui, 2009; Gao, Lam, & Wang, 2006; Habets & van Schuppen, 2002; Kotsalis, Megretski, & Dahleh, 2008; Kotsalis & Rantzer, 2010; Mazzi, Vincentelli, Balluchi, & Bicchi, 2008; Monshizadeh, Trentelman, & Camlibel, 2012; Shaker & Wisniewski, 2011; Zhang, Boukas, & Shi, 2009b; Zhang & Shi, 2008; Zhang, Shi, Boukas, & Wang, 2008). However, none of them deals with the problem addressed in this paper. The model reduction algorithm relying on a solution of LMIs is developed in Zhang, Boukas, and Shi (2009a) and further improved in Li, Lam, Gao, and Li (2014).

Outline In Section 2, we present the precise problem formulation. In Section 3, we present the fundamental theorem and corollaries, which form the basis of the reachability/observability reduction procedure for DTLSSs. The reduction algorithm is stated in
Section 4 in detail. Finally, in Section 5 the reduction procedure is illustrated on numerical examples.

Notation and terminology Denote by $|M|$ the cardinality of a set M, and by $\mathbb{N}$ the set of natural numbers including 0. Consider a non-empty set Q, which will be called the *alphabet*. Denote by Q^* the set of finite sequences of elements of Q. The elements of Q^* are called *words* over Q, and any set $L \subseteq Q^*$ is called a *language* over Q. Each non-empty word w is of the form $w = q_0 q_1 \cdots q_k$ for some $q_0, q_1, \ldots, q_k \in Q$, $k \geq 0$. In the following, if a word w is stated using q_is, e.g., $w = q_0 q_1 \cdots q_k$, it will be assumed that $q_0, q_1, \ldots, q_k \in Q$. The element q_i is called the $(i+1)$*th letter of* w, for $i = 0, 1, \ldots, k$ and $k+1$ is called the *length* of w. The *empty sequence (word)* is denoted by ε. The length of word w is denoted by $|w|$; note that $|\varepsilon| = 0$. The set of non-empty words is denoted by Q^+, i.e., $Q^+ = Q^* \setminus \{\varepsilon\}$. The *concatenation* of word $w \in Q^*$ with $v \in Q^*$ is denoted by wv: if $v = v_0 v_1 \cdots v_k$, and $w = w_0 w_1 \cdots w_m$, $k \geq 0, m \geq 0$, then $vw = v_0 v_1 \cdots v_k w_0 w_1 \cdots w_m$. If $v = \varepsilon$, then $wv = w$; if $w = \varepsilon$, then $wv = v$. In the sequel, the image and kernel of a real matrix M are denoted by $\mathrm{im}(M)$ and $\ker(M)$ respectively.

2. Problem formulation

Below, we present the formal definition of discrete time linear switched systems and recall a number of relevant definitions. We follow the presentation of Petreczky (2011) and Petreczky, Wisniewski, and Leth (2013).

Definition 1 (*DTLSS*)**.** A discrete time linear switched system (DTLSS) is a tuple

$$\Sigma = (p, m, n, Q, \{(A_q, B_q, C_q) | q \in Q\}, x_0), \tag{2}$$

where $Q = \{1, \ldots, D\}$, $D > 0$, is the set of discrete modes, $A_q \in \mathbb{R}^{n \times n}$, $B_q \in \mathbb{R}^{n \times m}$, $C_q \in \mathbb{R}^{p \times n}$ are the matrices of the linear system in mode $q \in Q$, and x_0 is the initial state. The number n is called the *dimension (order) of* Σ and will sometimes be denoted by $\dim(\Sigma)$.

Notation 1. *We use the following notation and terminology: The state space* $X = \mathbb{R}^n$*, the output space* $Y = \mathbb{R}^p$*, and the input space* $U = \mathbb{R}^m$*. We will write* $\overline{U^+ \times Q^+} = \{(u, \sigma) \in U^+ \times Q^+ \mid |u| = |\sigma|\}$*, and* $\sigma(t)$ *for the* $(t+1)$*th element* q_t *of a sequence* $\sigma = q_0 q_1 \cdots q_{|\sigma|-1} \in Q^+$ *(the same comment applies to the elements of* U^+, X^+ *and* Y^+*).*

A *solution* of the DTLSS Σ starting from the state $\hat{x} \in X$ and relative to the pair $(u, \sigma) \in \overline{U^+ \times Q^+}$ is a pair $(x, y) \in X^+ \times Y^+$, $|x| = |\sigma|+1$, $|y| = |\sigma|$ satisfying $x(t+1) = A_{\sigma(t)} x(t) + B_{\sigma(t)} u(t)$, $x(0) = \hat{x}$ and $y(t) = C_{\sigma(t)} x(t)$ for all $0 \leq t \leq |\sigma|$. Note that the pair $(u, \sigma) \in \overline{U^+ \times Q^+}$ can be considered as an input to the DTLSS.