Diamond & Related Materials 75 (2017) 78–84

Contents lists available at ScienceDirect

Diamond & Related Materials

journal homepage: www.elsevier.com/locate/diamond

Thin large area vertical Schottky barrier diamond diodes with low on-resistance made by ion-beam assisted lift-off technique

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ARTICLE INFO

Article history:
Received 16 November 2016
Received in revised form 6 February 2017
Accepted 6 February 2017
Available online 7 February 2017

Keywords:
Synthetic diamond
Schottky barrier diode
Ion beam implantation
Lift-off procedure
Forward current
Electrical properties

ABSTRACT

We designed and made 15 μm large area vertical Schottky barrier diamond diodes with resulting substrate thickness of about 1 μm. The ion-beam assisted lift-off technique was successfully used to separate 5×5 mm^2 active two-layered structure from ballast HPHT diamond substrate. The fabricated diodes had <6 mΩ$*$cm^2 (0.03 Ω) on-resistance at room temperature and 3 mΩ$*$cm^2 (0.015 Ω) at 200 °C fixed temperature of the diode case. A removal of large ballast substrate resistance results in a significant drop of on-state voltage, power losses and, therefore, increasing of diode efficiency. An additional technology step of sacrificial layer formation by ion implantation did not cause a considerable degradation of diode reverse characteristics. As a result, the room-temperature Baliga's figure of merit of the fabricated thin diodes is more than ten times higher comparing to earlier made thick diodes with a drift layer of the same thickness and boron content. 20 A maximum forward DC current and <2 V voltage drop were measured at fixed case temperatures in the range from 0 °C to 200 °C using an active heat sink.

1. Introduction

Wide band-gap semiconductors like GaN, AlN, SiC and diamond progress rapidly in high-power, high-frequency electronics due to strong demand for saving energy. Diamond possesses superior electrical, mechanical and thermal properties, but the technology of making diamond devices is less developed and just moves towards scalable manufacturing. Up to now Schottky barrier diodes (SBDs) with high breakdown voltage [1,2] or high current density [3] and having both good reverse and forward characteristics [4] have been made on synthetic diamond. However, despite the fact that the size of the single-crystal diamond wafer has been increased above 1 in [5], the most of the reported outstanding characteristics were measured on small size diodes with the Schottky contact area of about 0.01 mm^2 or less. The actual forward current for such devices was <1 A, even at a current density higher than 1 kA/cm^2. Thus the typical diamond based diodes cannot reveal benefits of this material when installed in practical power electronics circuits.

In contrast, the main goal of the current work was to realize diamond SBD capable for real high power operation. Recently we demonstrated a set of packaged vertical diamond Schottky barrier diodes with a crystal area up to 25 mm^2 using large high quality boron-doped IIb-type HPHT diamonds [6]. They had maximum forward current of 5 A and <0.2 Ω on-resistance [7]. The optimal operation temperature of diode crystal occurred 150–200 °C due to its self-heating at high forward current.

To improve SBD forward characteristics we fabricated two new designs with higher boron content in a drift layer to decrease its on-state resistance [8]. 10 A forward current in permanent mode was measured on these structures. However even in the case of two orders of magnitude higher boron concentration the on-resistance value reduced just 4 times, down to 0.05 Ω value at 200 °C temperature of diode case. At the same time the reverse voltages of such diodes degraded substantially. So the Baliga's Figure of Merit (BFOM) that counts the trade-off between the breakdown voltage and the on-resistance and indicates device high power performance, reduced [9].

The on-resistance of a diode characterizes its degree of perfectness. The ideal diode has zero on-resistance. In such a case its conduction power losses in on-state is minimal and depends linearly on V_{ON} parameter, which equals to zero in ideal diode as well. Real diodes have non-ideal IV-characteristic and non-zero power losses. The power losses of high-power diodes may be substantial, thus large cooling systems must be installed for heat dissipation. Reduction of the diode conduction power losses is one of the main tasks in diode design, particularly in the case of high-power diodes.

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http://dx.doi.org/10.1016/j.diamond.2017.02.006
0925-9635/

In vertical-type diodes the total on-state resistance is a sum of the active layer resistance, substrate resistance and ohmic contact resistance. In a case of diodes with highly doped active drift layer the substrate resistance dominates and must be reduced as much as possibly in order to decrease the total on-resistance.

The diamond substrate resistance can be reduced substantially by heavily boron-doping. However, an increase of boron content in HPHT IIb-type diamonds results in degradation of crystals quality due to an appearance of large number of extended defects such as staking faults, twin boundaries and dislocations [6,7]. Such defects in a substrate affects strongly on a quality of homoepitaxially grown drift layers that makes reverse characteristics of diode worse. Thus the density of dopant in the substrate cannot be very high.

Therefore the only way to reduce electrical (and thermal) resistance of boron-doped diamond substrate is its thickness reduction. However, mechanical making (polishing) of thin (tens microns) large enough HPHT diamond plates is very difficult. The aims of the present study were to employ ion-implantation assisted diamond lift-off method [10] to split the CVD drift layer from the HPHT substrate in order to minimize the substrate resistance and make thin vertical Schottky barrier diamond diodes with higher BFOM.

Applying this technique we reduced diamond substrate thickness down to about 1 μm and on-resistance to 0.03 Ω. The measured maximum forward current was 20 A. This method provides multiple use of a perfect single-crystal diamond billet for making a number of thin diodes with superior characteristics and reducing their fabrication costs.

2. Materials and fabrication procedure

In this study we used the same basic design and path for making vertical Schottky barrier diodes as previously [7,8]. The fabrication procedure was upgraded by supplement of substrate preliminary ion implantation to create buried defect layer under its surface and etching of this sacrificial layer after vacuum annealing to separate active epitaxial grown structure from HPHT substrate. Using this procedure thin diodes were made.

2.1. Buried defect layer formation

We employed High Voltage Engineering Europa B.V. air insulated electrostatic ion accelerator that provided ions with energy up to 500 keV. In order to define optimal experimental conditions we calculated implantation profiles by SRIM-2013 software package [11] for H^+, He^+ and C^+ ions. According to simulation results, light ions have longer stopping path in diamond and create a less subsurface damage than the equal beam energy more heavy ions, like carbon, for example (Fig. 1a). The last circumstance is very important for CVD growth of high quality epitaxial diamond layer on HPHT substrate after implantation. On the other hand, light ions require higher implantation dose which may cause blistering effect, i.e. formation of gas-filled cavities (bubbles) in solid matrix. This phenomenon is very typical for high-dose ion implantation into Si, Ge, GaAs and so on [12,13].

Blistering in diamond was described in several works [12,14–15] and it was found that unlike other semiconductor materials only implantation of hydrogen results in bubbles formation in diamond. Such an effect was not observed in deuterium or helium implanted samples. Possibly, it takes place due to very stiff diamond lattice where only hydrogen atoms are mobile enough to diffuse. The threshold dose for blistering effect was found to be ~5×10^{16} cm^{-2} that looks like a limit of hydrogen solubility in the implanted layer [16]. In contrast we estimated the total implantation dose of 10^{17} cm^{-2} required to exceed the typical diamond graphitization threshold value of about 10^{22} cm^{-3} [17].

So, to exclude blistering effect like in a case of hydrogen implantation and avoid much surface degradation like in a case of carbon ions we selected helium ions beam in our work. As it is shown in Fig. 1b, the ion energy increase results in a decrease of near surface damage. Thus the maximum possible implantation energy should be utilized for sacrificial layer formation. In this work the ion beam energy of 450 keV was limited by the highest long-term stable voltage of the accelerator. The total implantation dose of 10^{16} cm^{-2} was used to achieve recoils density in sacrificial buried layer slightly above the graphitization threshold.

To convert the buried defect layer into graphite-like sp^2-phase after implantation we annealed HPHT substrates in vacuum at 1400 °C during 30 min. Usually such transformation results in much increase in electrical conductivity and chemical etchability [18]. As was shown in [19] thermal annealing at moderate temperature like 800–1000 °C, typical for CVD growth process, resulted in partial graphitization of this layer and in formation of the nano-crystalline graphitic phase which was sandwiched between layers of tetrahedral amorphous carbon. The annealing temperature of at least 1400 °C is required to complete the graphitization of amorphous damage layer.

We inspected the effect of high temperature annealing of diamond substrate quality after ion implantation by Raman spectroscopy (Fig. 2). The Raman spectrum of as implanted samples was dominated by a broad peak with a maximum at about 1300 cm^{-1} (aside the residual diamond line originating from the underlying undamaged diamond), typical for amorphous sp^3-bonded carbon [20], and a broad peak at 1600 cm^{-1} which can be associated with different types of radiation induced defects. Vacuum annealing resulted in significant decrease of the shoulder in the Raman spectrum. Also we found that this treatment resulted in removing 1630 cm^{-1} component related to ⟨100⟩ split-

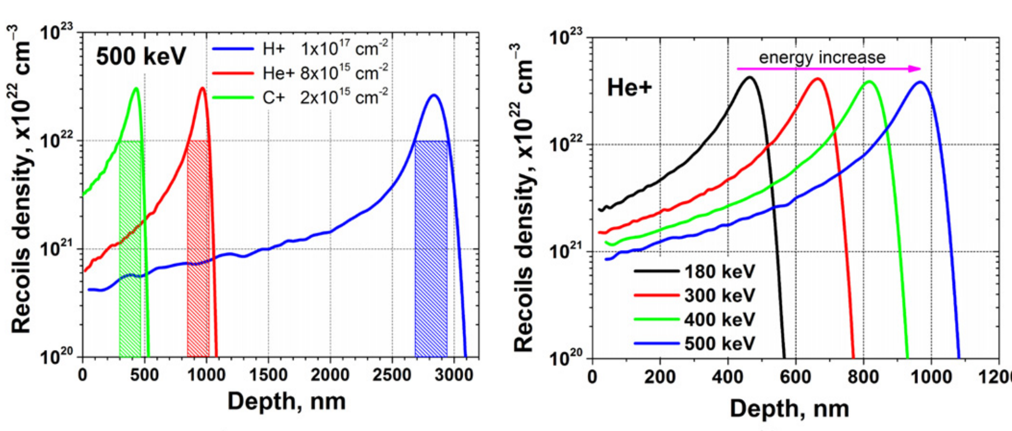

Fig. 1. SRIM simulation data for estimation of vacancies density in diamond during various implantation schemes: with different ions of fixed energy (a) and with He^+ ions varying their energy (b).