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A Study on Smart Fault Locator Based on Time-Synchronized Phasor

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Abstract: In order to reduce fault location estimation error, this paper deals with an enhanced fault location technique based on the improved DC offset filter. In addition, this paper presents the complete design of smart digital fault locator using GPS time-synchronized phasor. The smart fault location algorithm uses the transmitted relaying signals from the two-end terminal. The smart fault locator hardware consists of a main processor unit, analog to digital processor unit, signal interface unit, and power module. Various types of real-time test using COMTRADE format of Omicron apparatus are included.

Keywords: COMTRADE format, DC offset filter, GPS time-synchronized, Smart fault location algorithm, Transmission line, Two-end terminal

1. INTRODUCTION

Fault locators can help identify these locations for early repairs to prevent recurrence and consequent major damages in power system faults. The subject of fault location has been of considerable interest to power utility engineers and researchers for many years. Fault locators are used to quickly and accurately identify that the location for a fault has occurred in a line.

The main factors to consider in the fault locator are entering current through the fault resistance, influence of fault resistance, load current, presence of series and shunt in the line, inaccuracy in providing impedance, effect of zero sequence current at healthy line in parallel line, etc.

Methods of locating faults on power networks can be classified into two fundamental categories: techniques based on power frequency components, and the other utilizing the high-frequency components of the transient fault signals. Recently, a lot of research efforts have been focused on fault location techniques in line systems using intelligent technologies, such as artificial neural networks, fuzzy sets theory and expert systems.

Varieties of fault location algorithms have been developed so far. The majority of fault location algorithms are based on an impedance principle, making use of the fault locator input signals. During the phasor computation, the calculation error occurs due to the influence of the DC offset component. Therefore, fault location estimation error caused by transient vibration according to the measured impedance is generated.

This paper deals with an advanced fault location algorithm based on the improved DC offset elimination filter in order to reduce fault location estimation error. In addition, this paper presents the complete design of smart digital fault locator (sDFL) using GPS time-synchronized phasor. The smart fault location algorithm uses the transmitted relaying signals from the two-end terminal. The proposed algorithm was implemented on the smart digital fault locator. The sDFL hardware consists of a main processor unit, analog to digital processor unit, signal interface unit, and power module. Various types of real-time test using Common format for Transient Data Exchange for power systems (COMTRADE) format of Omicron apparatus are included.

2. SMART FAULT LOCATOR

2.1 Smart fault location algorithm

A conceptual diagram of the sDFL is shown in Fig. 1.

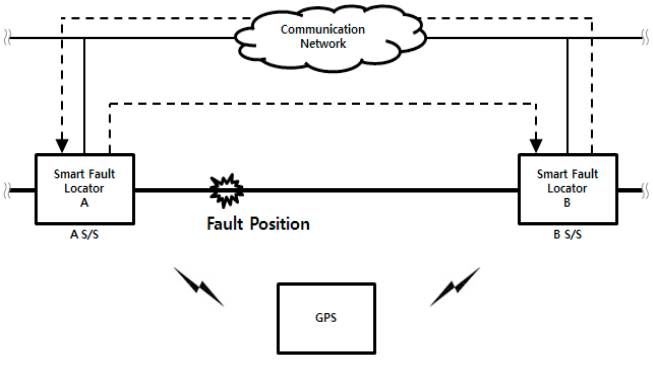

Fig. 1. Conceptual diagram of smart fault locator.

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We can see that smart fault location algorithm uses the transmitted relaying signals from two-end terminal using GPS time-synchronized phasor.
Two-end fault location algorithm is shown in Fig. 2. The fault distance calculation of the sDFL can be expressed as equation (1). It is calculated according to the distribution ratio of the impedance from two-end terminal.

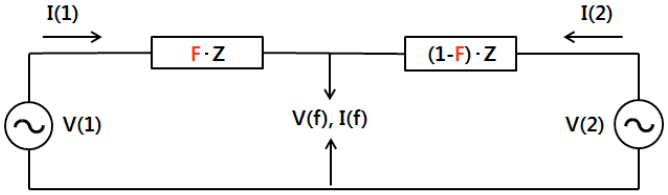

Fig. 2. Two-end fault location algorithm.

$$\mathrm{F} = \mathrm{Re}\left[\frac{\frac{V(1)-V(2)}{Z}+I(2)}{I(1)+I(2)}\right] \tag{1}$$

$$\mathrm{D} = F \cdot L$$

Where, $V(1), I(1), V(2), I(2), V(f), I(f)$ indicate GPS time-synchronized phasor measurement element, Z is line impedance, F is fault impedance ratio, and estimation fault distance is D.

2.2 DC offset filter algorithm

The improved DC offset filter from the fault current signal consisting of the DC offset component and harmonic components gradually removes DC offset component from the primary order harmonics to higher order harmonics, so the pure DC offset component remains. The DC offset component is subtracted from the error signals to achieve DC offset component filtering. The DC offset component in the fault signal can be determined by obtaining the initial value and the decaying rate of the DC offset.
The decaying rate and the initial value of DC offset can be expressed as equation (2) and equation (3).

$$D^S = \frac{\sum_{n=0}^{2^r-1} i[k+\frac{n}{2^r}N+s]}{\sum_{n=0}^{2^r-1} i[k+\frac{n}{2^r}N]} \quad \rightarrow \quad D = \sqrt[S]{D^S} \tag{2}$$

$$B = \frac{\sum_{n=0}^{2^r-1} i[k+\frac{n}{2^r}N]}{D^K \sum_{n=0}^{2^r-1} D^{\frac{n}{2^r}N}} \tag{3}$$

Where, initial value of DC offset is B, filter degree is r, sample number is k, decaying rate is D, and sampling per cycle is N.

2.3 Smart fault location hardware design

The sDFL hardware consists of four different boards, namely, a main processor unit (MPU), analog to digital processor unit (ADPU), signal interface unit (AIU), and power module. Modules of the sDFL and front view of the sDFL are shown in Fig. 3 and Fig. 4, respectively.

(a) MPU module

(b) SIU module

(c) ADPU module

(d) Power module

Fig. 3. Modules of smart fault locator.