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Zero Cross Detection Using Phase Locked Loop

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Abstract: This paper discusses zero cross detection method for the time synchronization purpose that is based on phase locked loop. After familiarizing with PLL concept and its blocks, example design of the PLL is realized. Simulation schema is introduced to examine and analyse PLL behaviour under different grid interferences. Performed tests show two potential issues multiple zero crossing in the zero cross area may cause instability of the loop and the presence of harmonics may cause shifts of the zero cross event.

Keywords: zero crossings, detection algorithms, phase-locked loop, grid interferences

1. INTRODUCTION

Zero crossing detection is one of the commonly used methods in electrical engineering, especially as a part of the frequency or period measurements. Other possible applications are signal phase measurement or direct use of zero crossing information, for example, as a part of controlled rectifier or triac phase regulator. In this paper, zero cross is intended to be used as a significant event for establishing of a common time base across PLC (power-line communication) devices connected to the grid that is usually achived by GPS nowdays (Slanina et al. (2011), Slanina et al. (2012)).

Many different technics are known for zero cross detection, starting with a simple low-pass filtering before detection, through rule-base technique that allow/block detection in certain time windows or linear interpolation across more samples and finishing with highly sophisticated technics with phase-locked loops or Fast Fourier transform.

This paper focuses on phase-locked loop utilization and possible issues with detection. The main idea is based on zero crossing detection that is performed at PLL output, not directly on the grid signal. PLL should eliminate different grid interferences like harmonics, notches, spikes or noise from signal, with its nature of operation. Zheng et al. (2015)

2. PRINCIPLE OF PHASE LOCKED LOOP

The phase locked loop is a feedback controlled circuit where the phase respectively frequency of the oscillator is internally controlled variable. This circuit (Fig. 1) consists of the phase detector, filter, voltage controlled oscillator (VCO) and selectable frequency divider. The principle is based on comparing the reference signal phase with the oscillator output. The difference is filtered and is used to control the VCO which subsequently adjusts its frequency what reduces the phase difference (Stensby (1997)).

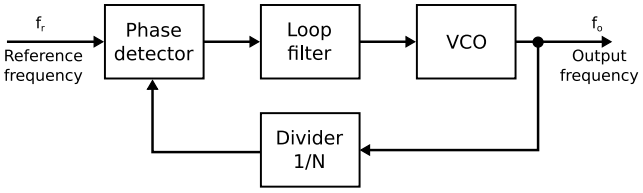

Fig. 1. Block diagram of the PLL

There are many realizations of the PLLs and the aim of this paper is not to describe them. However, the block diagram of the PLL is still the same, only the signal representation is changed (analogue or digital) or the blocks realization which differs according to technology or the approach. Next text will shortly describe the PLL blocks function for understanding of the concept (Gupta (1975)).

2.1 Phase Detector

The role of the phase detector is to determine a phase difference of signals. These signals are the reference signal and the feedback from the VCO. The phase detector output is used to control the VCO for the phase difference elimination. The phase detectors can be divided into two main groups: analogue and digital. For example, the analogue phase detector is a frequency mixer and the digital phase detector is a circuit with XOR gate or RS flip-flop. The important is the output characteristic of the detector, which could be periodic and aperiodic. The phase detector is divided into two groups (Barrett (1999)):

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- Phase detector - the output depends only on the phase of the signals.
- Phase-frequency detector - the output depends on the phase and the frequency.

The use of phase-frequency detector has a positive impact on the dynamics and overall parameters of the PLL because its output reflects also the frequency difference. Thanks to this PLL can significantly change the frequency when is irrelevant change the phase. This situation is mainly on big difference if the signal frequencies. This intervention must be filtered to achieve noise immunity.

2.2 Filtration

Filtration block, typically realized as low-pass filter, filters signal representing the phase difference of the reference and the VCO output. Its result is used to adjusting the VCO for reducing the phase difference to minimum. This filter affects the parameters of the PLL and its design is a compromise between PLL dynamics (lock speed) and noise immunity.

The main task of the filter is to determine the loop dynamic and therefore its stability. The PLL must remain stable on reference signal change, feedback divider change, PLL start-up or interference. The design should take into consideration the frequency operating range, PLL locking time, frequency change rate etc. The second task is peak suppression which can be generated by the phase detector. These peaks may cause oscillator modulation and reduce the quality of its spectrum.

2.3 Controlled Oscillator

The inevitable part of the PLL is the controlled oscillator. In case of the analogue realization, the output frequency is proportional to the input voltage. The digital PLL uses an oscillator, which is controlled by the digital information. The change rate is proportional to the input value. The oscillator output is connected back to the phase detector directly or through the feedback divider.

2.4 Feedback Divider

PLL may contain the feedback divider set between the oscillator and the phase detector. By setting the division coefficient to N is possible to create the signal with N-times higher frequency than the reference signal. With the second divider on the input of the reference signal is possible to generate frequency given by the ratio of these division factors. This method is often used to continuously change frequency to desired value only using the fixed reference oscillator.

3. PLL AND GRID INTERFERENCES

The primary problem to deal with in every detection method is the presence of interference in the analysed signal. The same applies if the analysed signal is the grid voltage where the customer can connect any device, in extremely inconvenient according to applicable technical standards. Also with the development of the renewable energy technologies, such as solar power plants where DC/AC inverters are used, the AC voltage is not generated by the rotating mass in the form of synchronous generators. All these factors have an adverse impact on the voltage waveform shape and indirectly affect requirements on detection method. Next chapter shows a simulation method for the PLL behaviour investigation under different effects of interferences (Liu et al. (2015), Arruda et al. (2001)).

Matlab-Simulink is used as the simulation environment where the simulation schematic was realized (Fig. 2). It consists of three main parts:

- Test signal generator - generates a signal with selectable interferences.
- Examined PLL - PLL exposed to interferences from the generator.
- Reference PLL - identical to examined PLL, but its input is an ideal sine signal.

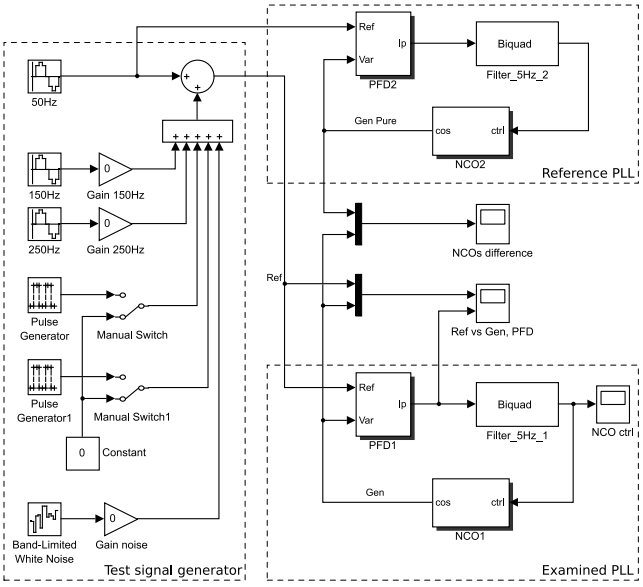

Fig. 2. Simulation schema for PLL verification

3.1 Signal Generator

Designed generator simulates a signal of the grid. It consists of the ideal 50 Hz sine signal source and the generator of several kinds of interference which parameters are described in individual test cases:

- Harmonic interference - simulation of 3rd a 5th harmonic in the grid
- Periodic pulses - simulation of the periodic pulsing interference
- Noise - white noise generator

Standard EN 50160 (European committee for standardization (2011)) defines the voltage characteristic of the distributed electric energy. The harmonics must not exceed the levels stated in Table 1 as the average value spread across time on all connecting terminals. Besides that, the total harmonic distortion (THD) (1) must not exceed 8 % as instantaneous value and 5 % as average value in 10 minutes and one week, respectively across all time. Three-phase grid voltage usually carries odd harmonics. In case