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# Digital equalizer for data acquisition path, constructed using IIR filters

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Abstract: The paper deals with method of designing of a digital equalizer for analog signal path with ADC and low-order low-pass filter on its front. The correction effect is achieved through use of the IIR digital filters, designed in equalization purposes of the magnitude frequency response. The application of an equalizer allows to gain high attenuation in cutoff band and expand the signal bandwidth. Simultaneously it allows using low order anti-aliasing analog filter on ADC front. The equalizer can operate as a separate device or could be build-in signal processor (or in any other signal processing ASIC). In the first case it could be prepared as a module, implemented in FPGA device.



*Keywords:* signal processing, signal correction, digital filters, IIR, ADC, FPGA

## 1. INTRODUCTION

In a typical circuit of analog data acquisition a compensation method is used very often (E. Balestrieri et al. (2005)). An acquisition channel consists of an analog low-pass filter *Fd*, sample and hold circuit (S/H) and analog to digital converter (ADC). The filter is applied for reduction of the processed signal bandwidth to the Nyquist frequency band (J.W. Leis (2011) and it makes the analog to digital processing unambiguous. Moreover, the sample and hold circuit should provide constancy of a input signal during operation of ADC converter, especially for using of the successive approximation register conversion – SAR ADC.

Data acquisition channel should not distort processed signals, i.e. it should has constant amplitude characteristics and linear phase characteristics. This means that the acquisition path should be a delay element and the output signal is delayed in reference to input one, but the waveform shapes of them are the same. Taking into account this feature, it is possible to build-in into the path an additional element – a digital equalizer. The purpose of this element is a modification of signals after conversion process. As a consequence, the correction effect is achieved, which allows for alteration of characteristics of channel's elements placed before the equalizer device. In this case it is a low-pass filter. In the example, which illustrates the discussed method, the 2nd order analog anti-aliasing filter was used. After correction the characteristic of circuit is adequate to the case where the 10th order filter was used.

The paper is organized as follow: in the next section informations related to analog signal correction are presented, next the data acquisition path for our methodology is introduced. Chapter 4 presents the method of designing of equaliser and in chapter 5 an example of equaliser is presented. Potential implementations of equaliser are given in chapter 6. The paper ends with conclusions.

## 2. ANALOG SIGNAL CORRECTION

The problem of the analog signal correction has been presented in the literature very often. The range of problems, potential applications and overviews of the techniques in this scope can be found in the works of S.V. Vaseghi (2013) and I. Pitas et al. (2013). The correction problem of analog data, where FIR filters were used is shown by I. Kollár and Y. Rolain (1993). Also some methods dedicated to ADC were proposed (P. Kiss et al. (2000)), in which the adaptive correction was performed on analog signals. More recent works in this scope are presented in a system of noise correction, reported in the form of a patent Asada and Itabashi (2015). The idea of digital correction is quite commonly present in issues related to DSP and digital acquisition paths. For example T.H. Tsai et al. (2006) and Y.C. Lim (2009) present bandwidth mismatch correction. Much of the work is devoted to the techniques of digital calibration (M.Seo et al. (2005)), also with the use of signal processing, presented in papers of S. Jamal et al. (2002), W. Namgoong (2002) and J. Pereira et al. (2004), where some solutions are consistent with the one presented in this article. However, in each of those cases, the presented solutions do not use the digital correction of analog filters as an inherent element of the data acquisition path.

## 3. DATA ACQUISITION PATH

Figure 1 illustrates a data acquisition channel. Note that the $F_d$ denotes a low-pass analog filter, and $G_{k_{(i)}}$ denotes transfer functions of components of corrector K. The parameters of individual elements of the path depend on a resolution, i.e. the number of bits and processing time. The resolution of ADC determines the maximal value of the harmonic component of the output signal of the filter, for frequency equal to half of the sampling frequency (H.S. Black (1953)). For example, in case of an 8-bit converter and frequency *fs*, the amplitude of the signal after filtering for the frequency *fs/2* should be 256 times less than the amplitude in the passband. This means that for a 2nd order filter, for which the slope of the amplitude beyond passband is 12 dB/octave – it


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corresponds to four times attenuation of signals for each twofold increase in frequency. The passband for the signal is about 16 times smaller than Nyquist frequency. For 10-bit ADC and 2nd order filter the passband should be 64 times less than Nyquist frequency. Due to the fact that the analysis of the signal in one channel, which contains equal amplitude harmonic components in the band of 2.5 kHz, for 10-bit converter with a fourth-order filter the sampling frequency should be at least 30kHz.

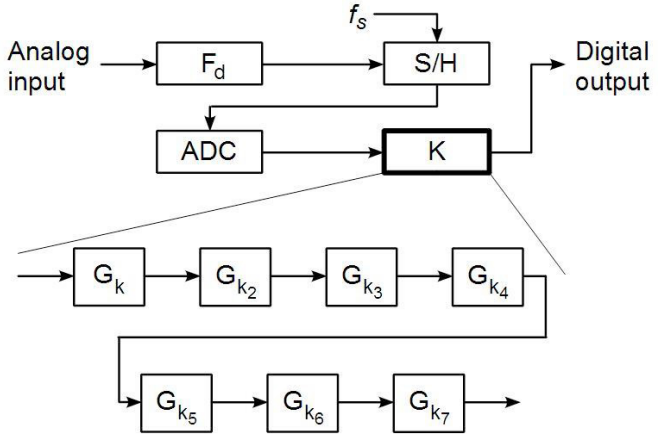


Fig. 1. *Data acquisition path with digital equaliser (K)*.

To avoid the use of high sampling frequency of analog signals, an expensive low-pass filters of a higher order should be used. In the case of multi-channel data acquisition, differences of parameters of filters in each channel may cause additional errors. Assuming that the passband and transition band of filters are the same, for 8-bit ADC 256-fold attenuation (about 48 dB) is required in the frequency range for one octave. This corresponds to at least eighth order of filter. That type of solution is complex and expensive, especially for resolution of ADC, which can be 12, 16 or even 24 bits (J. E. Johnston (2001)).

## 4. DESIGN OF EQUALIZER

In presented method for designing of data acquisition path the low-pass low order filter, adapted to resolution of ADC, is placed on S/H input. The S/H output is connected to ADC input. Next the equalizer is placed after S/H circuit – Fig. 1. The goal of equalizer is to compensate the characteristic of low-pass filter. Thus the equalizer expands the frequency range of the acquisition path. Also the equalizer compensates gain of filter in expanded frequency band and provides adequate attenuation of signal on digital part of acquisition circuit. The transfer function of this circuit is equal to product of the transfer functions of low-pass filter $G_{fd}(s)$ and equalizer $G_k(s)$. The S/H circuit as well as ADC provide only delay on signal, and do not affect the frequency characteristics of the entire system. Therefore the equalizer may compensate frequency characteristics of analog components (Fig. 1). The transfer function of low-pass filter is assumed as follow:

$$G_{fd}(s) = \frac{Y_{fd}(s)}{X(s)} = \frac{1}{A_0 \cdot s^2 + B_0 \cdot s + 1} \tag{1}$$

where $B_0 \geqslant \sqrt{2 \cdot A_0}$.

According to above method of choosing properties of equalizer, the denominator of transfer function (1) should be equal to the numerator of equalizer's transmittance. However, the equalizer circuit with the transfer function:

$$K(s) = \frac{1}{G_{fd}(s)} \tag{2}$$

after implementation in digital form is unstable – the equalizer begins oscillate, increasing amplitude until it exceeds the scope of permissible values. It is possible to obtain a stable operation of the equalizer through multiplying the equalizer's transmittance by function $W(s)$, which limits the bandwidth and makes the equalizer stable:

$$W(s) = \frac{1}{A_1 \cdot s^2 + B_1 \cdot s + 1} \tag{3}$$

where $B_1 \geqslant \sqrt{2 \cdot A_1}$.

Equation (3) is a low-pass filter transfer function, the parameters must be chosen so that the cut-off frequency is equal to the upper limit of the frequency response of the system after correction. The equalizer transfer function, determined in this way is the following:

$$K(s) = \frac{1}{G_{fd}(s)} \cdot W(s) = \frac{A_0 \cdot s^2 + B_0 \cdot s + 1}{1} \cdot \frac{1}{A_1 \cdot s^2 + B_1 \cdot s + 1} \tag{4}$$

Additionally, to reduce the transmission in stopband and improve the performance of the entire system, the extra low-pass filters should be used. The transfer function of those filters is given by equation:

$$F_{k_i}(s) = \frac{\left(\frac{A_{0_i}}{A_{1_i}}\right) \cdot \left(s^2 + \frac{B_{0_i}}{A_{0_i}} \cdot s + \frac{1}{A_{0_i}}\right)}{s^2 + \frac{B_{1_i}}{A_{1_i}} \cdot s + \frac{1}{A_{1_i}}}, i = 1,2,3\ldots \tag{5}$$

Finally the equalizer transfer function is defined as:

$$G_{k_i}(s) = \prod_{i=1}^{N} \quad F_{k_i}(s) \tag{6}$$

where: for $i$ = 1 relation (5) defines transmittance of equalizer $K(s)$, for $1 < i <$ N the additional filters transmittances are defined.

The equalizer circuit is based on analog prototypes, for which design process is presented in the previous section. Digital modules (6) are realized as units of infinite impulse response filters – IIR (C.S. Williams (1986)), characterized by a low computational cost – five multiplications and five summing operations is required for one unit. Parameters of particular units are determined on the basis of transfer function of analog prototype – the function $F_{k_i}(s)$, given in relation (5). Next, the Tustin's method (A.V. Oppenheim (1989)) is applied and function $F$ and it is transformed into a discrete form, where coefficient $B_0$ is given as:

$$B_0 = \frac{2 \cdot \pi \cdot f_0}{Q_0} \tag{7}$$